IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

SAMSUNG ELECTRONICS CO., LTD. AND SAMSUNG SEMICONDUCTOR, INC., Plaintiffs, v. NETLIST, INC., Defendant.	)	C.A. No. 21-1453 (RGA) (JLH) **PUBLIC VERSION**
NETLIST, INC., Counterclaim-Plaintiff, v. GOOGLE LLC, ALPHABET INC., SAMSUNG ELECTRONICS CO., LTD., AND SAMSUNG SEMICONDUCTOR, INC., Counterclaim-Defendants.	)	

JOINT CLAIM CONSTRUCTION BRIEF

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Samsung Electronics Co., Ltd.; Samsung Semiconductor, Inc.; Google LLC; Alphabet Inc.; and Netlist, Inc. respectfully submit this Joint Claim Construction Brief.

I. Introduction

A. Netlist's Statement

Plaintiff Netlist, Inc. ("Netlist") respectfully submits this opening claim construction brief on U.S. Patent No. 10,217,523. Ex. 1.[1]

1. Background

The products accused of infringement in this case are DDR4 LRDIMMs manufactured outside of the United States by Samsung[2,3] and imported and/or sold in the United States by at least Google and Samsung. [redacted]

[redacted]

Ex. 40 at 4. In 2008, Netlist presented under NDA its LRDIMM design to Samsung. This is the design described as one of the embodiments of the '523 patent:

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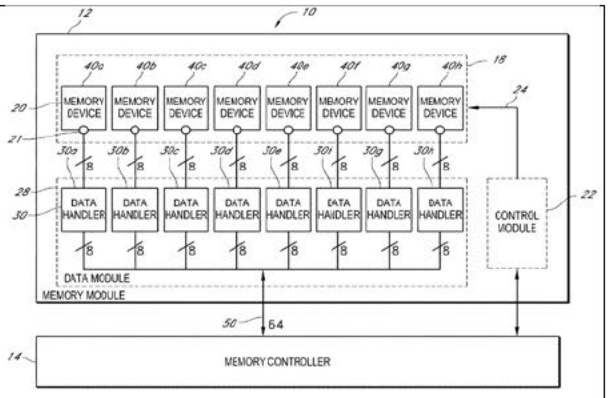
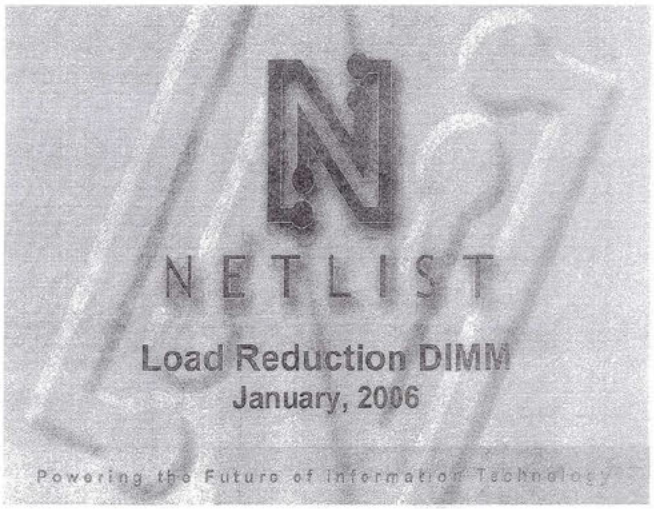
[1] Netlist has asked the court to sever and stay the claims of U.S. Patent Nos. 9,858,218 and 10,474,595 in light of the PTAB's decision to invalidate the asserted claims of those patents, which is pending appeal.

[2] Counter-Defendants Samsung Electronics Co., Ltd., and Samsung Semiconductor, Inc., are referred to collectively as "Samsung." Counter-Defendants Google LLC and Alphabet Inc. are referred to collectively as "Google."

[3] [redacted]

[redacted]	
Ex. 42 (October 2008, "DXD/LRD DRAM Partnership Program," presented under NDA to Samsung) at 17.	Ex. 1 ('523 Patent), Fig. 2.

Google, likewise, has long been focused on using Netlist's expertise in LRDIMMs. In a 2006 presentation, Netlist provided Google with information on its design program for LRDIMMs. Google ultimately chose to commission LRDIMMs from Samsung:



See Ex. 41.

2. PTAB Proceedings

Samsung challenged the validity of all asserted claims in the PTAB. The PTAB rejected all of these challenges and held the claims not unpatentable. Ex. 28 (Final Written Decision,

IPR2022-00063). In a number of instances, Samsung/Google are taking positions before this Court entirely inconsistent with positions taken before the PTAB.

3. Statement in Reply

Defendants' random quotation of passages from briefs and declarations involving different patents has claim construction entirely backwards. Claim construction begins with the claim language in the actual patent at issue before this Court, and it is this claim language that holds primacy. "[T]he claim construction inquiry . . . begins and ends in all cases with the actual words of the claim." *Homeland Housewares, LLC v. Whirlpool Corp.*, 865 F.3d 1372, 1375 (Fed. Cir. 2017). And extrinsic evidence cannot alter the meaning of terms as evidenced by the plain language of the claims and the intrinsic record. *Profectus Tech. LLC v. Huawei Techs. Co.*, 823 F.3d 1375, 1380 (Fed. Cir. 2016) ("Extrinsic evidence may not be used 'to contradict claim meaning that is unambiguous in light of the intrinsic evidence.'").

B. Samsung and Google's Statement

The '523 patent "relates to self-testing electronic modules and, more particularly, to self-testing electronic memory modules." '523 patent at 1:31–34. To avoid the potential failure of memory components—and ensuing loss of data—"[m]emory integrated circuits ('memory chips') often go through a series of tests at various stages of system manufacture . . . for memory defects and for the correct operation of the input/output interface." *Id*. at 1:41–43, 1:50–51.

According to the '523 patent, "the usefulness of" prior testing methodologies was "limited due to the high cost and other limitations." *Id*. at 2:6–8. In particular, "external test hardware . . . [was] very expensive." *Id*. at 2:8–10. The alleged solution presented by the '523 patent is a module that self-tests, internally generating test signals and data within the memory module that allegedly reduce or avoid these high costs. *See id*. at 2:4–3:6, 3:32–49; Figs 3, 5. Figure 3, reproduced below, illustrates how this self-testing process of the '523 works.

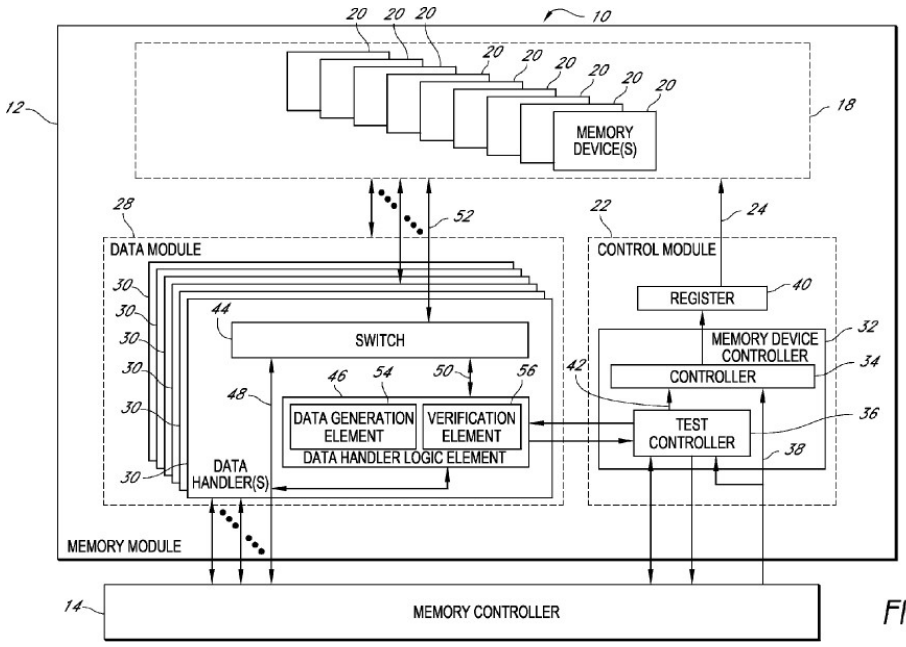


FIG. 3

The memory module in this system includes a printed circuit board coupled to a memory controller of a computer system. *Id*. at 5:4–12. The memory module has numerous memory devices, with each memory device comprising data, address, and control ports. *Id*. at 5:8–12. The memory module further has a control module and a data module. *Id*. at 5:12–16. The data module, in turn, comprises numerous data handlers that "may be operatively coupled to (*e.g.*, logically and/or electrically coupled to) the corresponding plurality of data ports" of the memory devices. *Id*. at 5:19–23. Each of these data handlers includes a data handler logic element, comprising a data generation element and a verification element. *Id*. at 10:37–40.

The '523 patent discloses two modes of operation for the module: a "normal mode" and a "test mode." *Id*. at 2:38–40; *see also, e.g.*, *id*. at 9:55–60, 13:59–14:4. In the normal (non-test) mode, the system memory controller (the server) writes or reads data to the memory module. *See e.g., id*. at 2:40–45, 3:63–77, 10:26–31, 15:3–12; Ex. 11 (Brogioli Decl.), ¶ 30. In the test mode, the data handlers generate data patterns that are sent to the memory devices, as discussed above. *See, e.g., id.* at 5:66–6:7, 6:3–7, 15:13–30; Ex. 11 (Brogioli Decl.), ¶ 30. The specification further

explains that in the test mode, the "data generation element" on the data handler logic element "may be configured to generate data signals (e.g., patterns of data signals) for writing to the corresponding plurality of data ports" of memory devices. *Id.* at 10:41–43. In sum, as Netlist's expert opines, "[t]he '523 patent relates to . . . a self-testing architecture for memory modules that utilizes certain on-board components to conduct testing functions 'without substantial system memory controller involvement.'" Ex. 11 (Brogioli Decl.), ¶ 30.

Over the past decade, Netlist has engaged in a widespread litigation campaign against suppliers of JEDEC standard-compliant memory modules, such as Samsung, and their customers, such as Google. As part of that campaign, Netlist previously asserted three patents that share a specification with the '523 patent at issue here. After years of litigation, not a single Netlist patent claim was found valid and not a single claim infringed. As set out below, Netlist now attempts to read its claims broadly, divorced from the intrinsic evidence that defines the alleged invention, contrary to Netlist's binding admissions, and dismissive of prior claim construction rulings.

II. Agreed-Upon Constructions

Term, Clause, or Phrase	Agreed Construction
"A memory module accessible in a computer system by a system memory controller via a system memory bus, comprising" (cl. 1)	The preamble is limiting.
"A memory module operable in a computer system with a system memory controller, the memory module comprising" (cl. 19)	The preamble is limiting.
"memory device[s]" (cls. 1–4, 9, 10, 12, 15, 16, 19–34)	memory integrated circuits

III. Disputed Constructions

A. "memory module" (cls. 1–34)

Samsung & Google's Proposed Construction	Netlist's Proposed Construction

"printed circuit board on which memory integrated circuits are mounted"	plain and ordinary meaning, limiting preamble, a memory module needs to include structures necessary to connect to a memory controller

1. Netlist's Opening Position

The preambles of independent claims 1 and 19 claim a memory module accessible by (or operable with) a memory controller, thereby presuming that a "memory module" includes structures necessary to form a functioning connection with a memory controller. The preambles of claims 1 and 19 state:

> 1. A memory module accessible in a computer system by a system memory controller via a system memory bus . . .
> 19. A memory module operable in a computer system with a system memory controller . . . .

Ex. 1 ('523 Patent) at cls. 1, 19. Claiming a "module X" connected to "controller Y" necessarily implies that "module X" has the structures in place to make the connection with "controller Y" work.

During prosecution, Netlist distinguished prior art on the basis that it describes a microprocessor with embedded memory units in contrast to a memory module:

> Zuraski in view of Jacob does not disclose the memory module in claim 1. First of all, Zuraski does not even disclose a memory module. A memory module is a printed circuit board on which memory integrated circuits (memory devices) are mounted (http://en.wikipedia.org/wiki/Memory_module; also, Specification paragraph [0024] and FIG 1). Zuraski, on the other hand, is all about a microprocessor 10, which is not a memory module. A microprocessor is a computer processor which incorporates the functions of a computer's central processing unit (CPU) on a single integrated circuit (IC) . . . . Ex. 5 (2016-07-11 Amendment & Responses) at 17-18 (emphasis in original).

Although the description of a memory module used in the exchange is accurate, it is incomplete as the term is used in the claims. The PCB must be able to electrically communicate with the memory controller. Paragraph [0024] and Figure 1 of the patent application make this clear as well. Ex. 3 (14/229,844 Patent Application) at 6-7 ("The memory module 10 includes a printed

circuit board 12 ***configured to be operatively coupled to a memory controller 14*** of a computer system 16."), 40 (emphasis added); *see also* Ex. 1 ('523 Patent) at Fig. 1, 5:4-27.

2. Samsung and Google's Answering Position

All of the asserted claims of the '523 patent require a "memory module." The intrinsic evidence supports and requires Samsung and Google's construction that a "memory module" is a "printed circuit board on which memory integrated circuits are mounted."

Samsung and Google's construction comes directly from the applicant's own explicit definition of "memory module" when the applicant distinguished the invention from the prior art. In a March 9, 2016 Office Action, the examiner rejected then-pending claims 1–25 under 35 U.S.C. § 103 as being unpatentable over Zuraski (U.S. Patent No. 6,650,740) in view of Jacob ("Synchronous DRAM Architectures, Organizations and Alternative Technologies, 12/10/2002"). Ex. 4 ['523 FH, March 9, 2016 Office Action] at 10–12. To traverse this rejection, the applicant sought to distinguish the Zuraski and Jacob combination on the basis that Zuraski did not disclose a "memory module":

> Zuraski in view of Jacob does not disclose the memory module in claim 1. First of all, Zuraski does not even disclose a memory module. A memory module is a printed circuit board on which memory integrated circuits (memory devices) are mounted (https://en.wikipedia.org/wiki/Memory_module; also, Specification, paragraph [0024] and FIG. 1). Zuraski, on the other hand, is all about a microprocessor 10, which is not a memory module. A microprocessor is a computer processor which incorporates the functions of a computer's central processing unit (CPU) on a single integrated circuit (IC)

Ex. 5 ['523 FH, July 11, 2016 Response] at 17. In doing so, the applicant explicitly defined the "memory module" of the '523 patent as a "printed circuit board on which memory integrated

circuits (memory devices) are mounted." *Id.* This definition is binding as a matter of law.[4] *See Nystrom v. TREX Co., Inc.*, 424 F.3d 1136, 1144 (Fed. Cir. 2005) (construing "board" consistent with applicant's definition of "board" during prosecution); *see also Tech. Properties Ltd. LLC v. Huawei Techs. Co.,* 849 F.3d 1349, 1359 (Fed. Cir. 2017) (holding that narrowing construction "properly encapsulate[d] the patentee's disclaiming statements" distinguishing over prior art reference); *Gemalto SA v. HTC Corp.*, 754 F.3d 1364, 1371–72 (Fed. Cir. 2014) (limiting construction of "memory" to "all program memory," which means "sufficient memory to run the Java code" and excluding "off-chip memory" based on statements the applicant made disclaiming external memory sources during reexamination of the asserted patent).

In making this binding statement, the applicant cited column 5:4–26 in the '523 specification (corresponding to paragraph [0024] in the application) and Figure 1. Ex. 5 ['523 FH, July 11, 2016 Response] at 17. This portion of the specification states, in relevant part:

> FIG. 1 is a block diagram of an example self-testing memory module 10 in accordance with certain embodiments described herein. ***The memory module 10 includes a printed circuit board 12*** configured to be operatively coupled to a memory controller 14 of a computer system 16. The ***memory module 10 further includes a plurality of memory devices 18 on the printed circuit board (PCB) 12*** . . . .

'523 patent at 5:4–10 (emphasis added). Thus, the specification further confirms (as the applicant acknowledged) that the "memory module" is a printed circuit board on which memory integrated circuits (*e.g.*, "a plurality of memory devices" and "memory controller") are mounted. Samsung and Google's construction is also consistent with how "memory module" is defined in U.S. Patent No. 8,154,901, which is part of the same family and claims priority from the same provisional

[4] Notably, Netlist agrees with Samsung and Google's proposed construction that "memory device" is a "memory integrated circuit" as defined in this same portion of the prosecution history (*see* highlights in the above excerpt). D.I. 145 [Joint Claim Construction Chart]; Ex. 5 ['523 FH, July 11, 2016 Response] at 17.

application as the '523 patent. Ex. 2 ['901 patent] at 2:17–19 ("The memory module comprises a plurality of memory devices on the printed circuit board and a circuit.").

The applicant's binding construction of "memory module" is further consistent with the additional support that the applicant cited for this definition during prosecution. Ex. 5 ['523 FH, July 11, 2016 Response] at 17. For example, the applicant cited Wikipedia, which still says "a memory module or RAM (random-access memory) stick is a *printed circuit board on which memory integrated circuits are mounted*." *Memory Module*, Wikipedia, https://en.wikipedia.org/wiki/Memory_module (last visited Aug. 28, 2023) (emphasis added).

In other litigation, Netlist has relied on similar definitions of "memory module." For example, in *Netlist, Inc. v. SK Hynix Inc., et al*, 8:16-cv-01605-JLS-JCG (C.D. Cal.), when arguing the construction of the same term in Netlist's U.S. Patent No. 8,489,837, Netlist pointed to "industry-trusted encyclopedias and text" that define "memory module," consistent with Samsung and Google's construction. Ex. 14 [NL Opening *Markman* Brief] at NL-SS-1453_00061386, *citing* Freedman, Alan, Computer Desktop Encyclopedia, 9th Ed., p. 596 (defining "memory module" as "a narrow printed circuit board that holds memory chips, typically dynamic RAM (DRAM) or synchronous dynamic RAM (SDRAM) . . . ."); Jacobs et. al., Memory Systems: Cache, DRAM, Disk, pp. 315, 319 (defining "memory module" as "the small computer board (a printed circuit board, or PCB) that has a handful of chips attached to it."); *see also* Ex. 15 [William Mangione-Smith Decl.] at NL-SS-1453_00061360 (citing same definitions).

Netlist cites the same portion of the prosecution history discussed above, and says it is "accurate," but "incomplete." *Supra* at 6. Initially, if what the prosecution history says is "accurate," there should no reason not to construe the term consistent with the prosecution history, as required as a matter of law. Nor does Netlist explain how the definition required by the

prosecution history is "incomplete," or why it provided an "incomplete" definition to the Patent Office. While Netlist says, as its construction recites, that "a memory module needs to include structures necessary to connect to a memory controller," Samsung and Google's construction allows for that and *does not preclude* these supposedly necessary "structures." Indeed, this is shown by Netlist's own citation to the patent application. *Supra* at 6–7 (citing Ex. 3 (14/229,844 Patent Application at 6–7). This language says "[t]he memory module 10 includes a printed circuit board 12 configured to be operatively coupled to a memory controller 14 of a computer system 16." This is the same "printed circuit board" in Samsung and Google's construction. Netlist is creating a strawman to sidestep the required construction from the prosecution history that it concedes is "accurate." Netlist cannot do so as a matter of law. *See Omega Eng'g., Inc. v. Raytek Corp*., 334 F.3d 1314, 1323–24 (Fed. Cir. 2003) ("The doctrine of prosecution disclaimer . . . preclud[es] patentees from recapturing through claim interpretation specific meanings disclaimed during prosecution."); *SpeedTrack, Inc. v. Amazon.com*, 998 F.3d 1373, 1379 (Fed. Cir. 2021) ("An applicant's argument that a prior art reference is distinguishable on a particular ground can serve as a disclaimer of claim scope even if the applicant distinguishes the reference on other grounds as well.").

3. Netlist's Reply Position

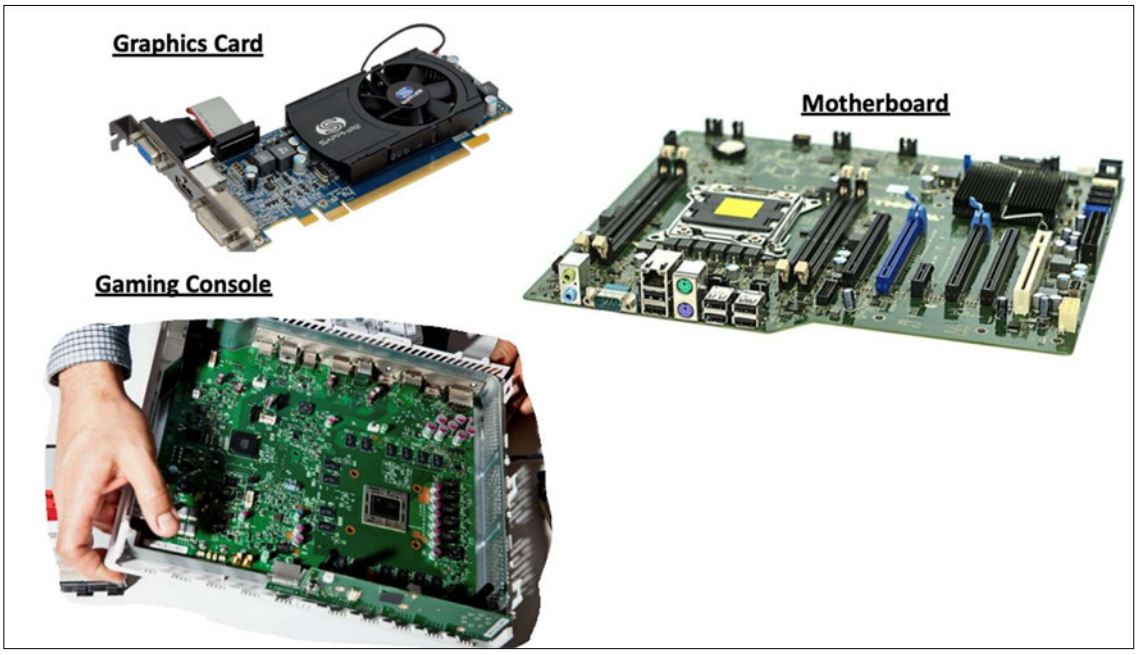
The preamble is limiting. It recites a memory module that is "accessible . . . by a system memory controller via a system memory bus." The pre-amble provides the antecedent basis for the subsequent reference to "**the** system memory bus" and "**the** system memory controller." *Shoes by Firebug LLC v. Stride Rite Children's Grp.*, LLC, 962 F.3d 1362, 1367 (Fed. Cir. 2020) ("[D]ependence on a particular disputed preamble phrase for antecedent basis may limit claim scope . . ."). The preamble makes clear that the inventive device is connected to an off-module memory controller.

The Defendants plan to argue at a later point in this litigation that a memory module need not include structures necessary for the memory devices to connect to a memory controller. The portions of the specification the Defendants cite in support of their construction confirm that a memory module includes structures sufficient to connect to a memory module:

> FIG. 1 is a block diagram of an example self-testing memory module 10 in accordance with certain embodiments described herein. ***The memory module 10 includes a printed circuit board 12*** configured to be operatively coupled to a memory controller 14 of a computer system 16. The ***memory module 10 further includes a plurality of memory devices 18 on the printed circuit board (PCB) 12***

Supra at 8 (yellow highlight added by Netlist to show the relevant portion of the specification ignored by Defendants).

Defendants argue that their proposed construction "allows for . . . and *does not preclude* these supposedly necessary 'structures.'" *Supra* at 10. The problem is that the proposed construction also allows the Defendants to argue that motherboards, graphics cards, gaming consoles, cell phones, and laptop computers all qualify as memory modules because they comprise PCBs with memory mounted on them.



Contrast this with "memory modules" as described in the patent: in every instance, the specification teaches that they are designed to communicate with an off-module memory controller. It is this feature that distinguishes the "memory module" from all of the above random computer-related devices that have a PCB and memory.

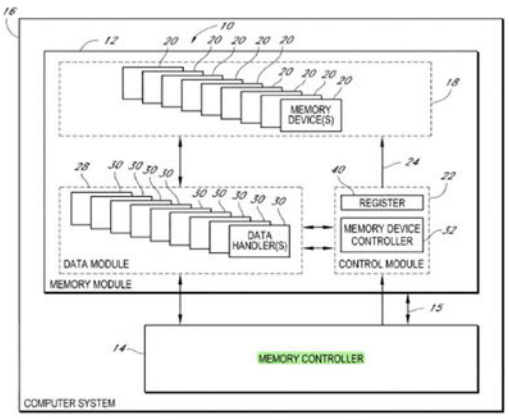


FIG. 1

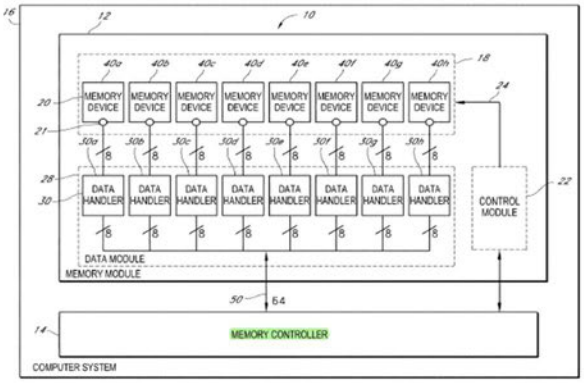


FIG. 2

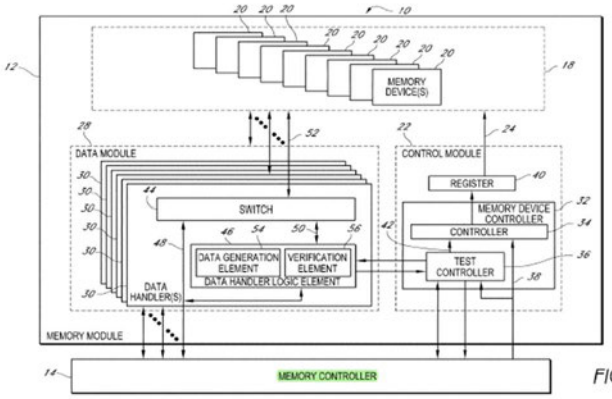


FIG. 3

See also '523, Abstract, Summary (2:31-47; 2:48-58; 2:63-3:6); Detailed Description (5:4-8, 7:1-7, 7:30-51, 8:49-53, 10:7-10, 12:63-66; 13:25-27; 16:55-57; 19:4-6).

The prosecution statement on memory module, based on a Wikipedia definition, is accurate but incomplete. It is incomplete because the issue before the PTO was whether Zuraski's microprocessor with embedded memory qualified as a memory module. As such, Netlist's statements emphasized the "printed circuit board" and "mounted memory devices" aspects to make

the distinction. The question of whether a memory module could encompass a design that was not operatively coupled to a memory controller of a computer system was not joined:

> Zuraski in view of Jacob does not disclose the memory module in claim 1. First of all, Zuraski does not even disclose a memory module. A memory module is a printed circuit board on which memory integrated circuits (memory devices) are mounted (http://en.wikipedia.org/wiki/Memory_module; also, Specification paragraph [0024] and FIG 1). Zuraski, on the other hand, is all about a microprocessor 10, which is not a memory module. A microprocessor is a computer processor which incorporates the functions of a computer's central processing unit (CPU) on a single integrated circuit (IC) . . . . **As such, the microprocessor 10 in Zuraski has embedded memory units 16a-16b** (Zuraski, FIG. 1, and col. 5, line 50, emphasis added). **These embedded memory units 16a-b are memory cells embedded in the microprocessor integrated circuit** (Zuraski, col. 6, lines 48-52) **and do not include the mechanisms (e.g., the input/output circuits and proper packaging) for mounting on a circuit board** (Zuraski, col. 6, lines 48-64). . . . **[A] person of ordinary skill in the art could not possibly be motivated to adopt the teachings of Jacob by taking the embedded memory units 16 out of Zuraski's microprocessor 10 and mount them onto a circuit board**.

Ex. 5 at 18-19 (emphasis added). Netlist's prosecution statements were directed to contrasting *mounting* with *embedding* of memories and did not purport to definitively construe the term "memory module." Distinguishing a claim over prior art in prosecution based on one feature does not preclude the fact that there may be additional differences.

Defendants' string-cited prosecution disclaimer cases are inapposite because they involve situations where a patentee attempted to "recaptur[e] through claim interpretation specific meanings disclaimed during prosecution." *Supra* at 10 (citing *Omega Eng'g., Inc. v. Raytek Corp*., 334 F.3d 1314, 1323–24 (Fed. Cir. 2003)). In all those cases, the patentee distinguished prior art on a particular basis but later advanced a *contradictory* construction that would recapture the disclaimed subject matter. *See Nystrom v. TREX Co.*, 424 F.3d 1136 (Fed. Cir. 2005) (during prosecution, patentee distinguished non-wood material but later advanced construction that would encompass such materials); *Tech. Properties Ltd. LLC v. Huawei Techs. Co.*, 849 F.3d 1349, 1358–59 (Fed. Cir. 2017) (during prosecution, patentee distinguished fixed-frequency crystal

oscillator and external crystal or frequency generator, but later sought construction that would read on such products); *Gemalto S.A. v. HTC Corp.*, 754 F.3d 1364, 1369–70 (Fed. Cir. 2014) (during prosecution, patentee distinguished prior art by emphasizing the novelty of squeezing a Java application onto the memory of an integrated circuit card, but later).

In contrast, to the extent the prosecution statement on the "memory module" is construed as a disclaimer against microprocessors with embedded memories, Netlist is *not* attempting to reclaim this subject matter. Instead, Netlist's proposed construction does nothing more than reflect what is required by the pre-amble, which does not just recite a memory module but recites that it is communicating with a memory controller off module.

The extrinsic evidence cited does not undermine Netlist's position. First, the Wikipedia article states that "a memory module . . . is a printed circuit board on which memory integrated circuits are mounted," but all the example modules depicted or discussed include structures that enable connection to a memory controller. Ex. 44. Additionally, the article cites the treatise *Memory Systems: Cache, DRAM, Disk* ("Jacobs," Ex. 45) as support, which Defendants have also cited in their brief. *Supra* at 9. Citing Jacobs, the court in *Samsung I* concluded that memory modules include structures necessary to connect to a memory controller:

> [A] skilled artisan would understand a "memory module" is distinct from, and has essential structural requirements not necessarily found in, other modular computer accessories. That **includes the structure necessary to connect to a memory controller.** *See Memory Systems: Cache, DRAM, Disk*, Dkt. No. 76-17 at 319 (depicting, in FIG. 7.6, a memory controller connected to two memory modules).

Ex. 18 (Markman Order, Dkt. 114, *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al*, 2:21-cv-00463 (E.D. Tex.)) at 28 (emphasis added).

The full context of U.S. Patent No. 8,154,901 cited by Defendants also supports Netlist's construction and undermines Defendants. That patent states:

> Certain embodiments described herein include **a memory module comprising a printed circuit board *comprising at least one connector configured to be operatively coupled to a memory controller of a computer system*.** The memory module comprises a plurality of memory devices on the printed circuit board and a circuit.

'901, 2:14-19. Defendants' citation omits the first sentence that makes clear that the claimed memory module, in that case, includes structures necessary to connect to a memory controller.

Defendants' citations to proposed constructions in a past case pertaining to unrelated U.S. Patent 8,489,837, with a different specification and prosecution history, cannot overcome the plain language of the claims. *See SIPCO, LLC v. Emerson Elec. Co.*, 980 F.3d 865, 870 (Fed. Cir. 2020) (holding that a prior case did not constrain the court's claim construction analysis because, "[i]mportantly, that case involved different patents, in entirely different patent families, with different specifications").

4. Samsung and Google's Sur-Reply Position

Netlist's reply does not substantively rebut the overwhelming evidence requiring Samsung and Google's construction. Instead, Netlist raises a strawman that "Defendants plan to argue at a later point in this litigation that a memory module need ***not*** include structures necessary for the memory devices to connect to a memory controller." There is no support for this conjecture. To the contrary, Samsung and Google's construction *permits* structures that "enable connection to a memory controller." Netlist contends that "the problem" with Samsung and Google's construction is that it encompasses devices that indisputably are not "memory modules." It is unclear what the "problem" is here, given that the same is true for Netlist's own construction.

Netlist does not dispute that Samsung and Google's construction is based on the applicant's explicit definition of "memory module" in the prosecution history. This is binding on Netlist as a matter of law. *Supra* at 7–8, 10 (collecting cases). Netlist contends the cases cited by Samsung and Google are irrelevant because in those cases "the patentee distinguished prior art on a particular

basis but later advanced a *contradictory* construction that would recapture the disclaimed subject matter." But that is exactly the case here—Netlist distinguished Zuraski by defining "memory module" to require the "mounting" of integrated circuits on a PCB, and Netlist is now advancing a contradictory interpretation of "memory module."

What Netlist really seems to be arguing is that it did not ***need*** to provide the specific definition in order to distinguish Zuraski. But that is irrelevant as a matter of law. *See, e.g.*, *Tech. Properties Ltd. LLC v. Huawei Tech. Co., Ltd.*, 849 F.3d 1349, 1358 (Fed. Cir. 2017) ("[T]he scope of surrender is not limited to what is absolutely necessary to avoid a prior art reference; patentees may surrender more than necessary."). In any event, if not somehow a disclaimer, it is well settled that a patentee can choose to be his own lexicographer by clearly setting forth a definition for a term in the prosecution history and expressing an intent to redefine the term. *See, e.g.*, *Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014). Here, Netlist expressly and intentionally defined "memory module" and ***also*** disclaimed any broader interpretation.

Netlist's argument as to the "extrinsic" evidence fails. Netlist contends that the Wikipedia article cited in the prosecution history "does not undermine" Netlist's position. Not so. The applicant's definition of memory module, with a citation to Wikipedia, is ***intrinsic*** evidence because it is part of the prosecution history. In any event, Netlist merely argues that "the example modules depicted or discussed [in Wikipedia] include structures that enable connection to a memory controller." But Netlist does not dispute that Samsung and Google's construction—taken directly from the same Wikipedia portion—***also*** allows structures that "enable connection to a memory controller." If anything, Netlist's argument demonstrates that Samsung and Google's construction is accurate and complete, not "incomplete" as Netlist concludes without support. Netlist's attempt to explain away the definitions of "memory module" in Jacobs et. al., Memory

Systems: Cache, DRAM, Disk, and Netlist's U.S. Patent No. 8,154,901 fails for similar reasons.

B. "first mode" / "second mode"

Samsung & Google's Proposed Construction	Netlist's Proposed Construction
"first mode" (cls. 1, 2, 19, 20)	
"normal (non-test) mode"	plain and ordinary meaning, a mode that differs from the "second" mode
"second mode" (cls. 1, 4, 11, 19, 20, 24, 30, 32)	
"self-test mode"	plain and ordinary meaning, a mode that differs from the "first" mode

1. Netlist's Opening Position

Before the PTAB, Samsung sought to have the term "mode" construed as plain and ordinary mean. Ex. 19 (Petition, IPR2022-00063) at 14. Netlist had historically proposed that a "mode" is "a distinct behavioral state that a system may be switch to." *Id.* Samsung argued that "[t]he intrinsic record never defines "*mode*" or uses it in any special sense, so the Board should take the same approach here." *Id.* Samsung did not seek construction of "first mode" and "second mode." *See id.* Ultimately, the PTAB did not adopt a particular construction of "mode." *See* Ex. 28 (FWD, IPR2022-00063) at 11-12.

The plain language of the claims defines the "first mode" and the "second mode." Independent Claim 1 states that the control module in the "first mode" must be:

> configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals

Ex. 1 ('523 Patent) at cl. 1. Likewise, the data module in the "first mode" must be:

> configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals

Id. Similarly, independent Claim 1 also sets forth that the control module in the "second mode" must be "configured to output second memory address and control signals to the address and control ports of the memory devices." *Id.* Finally, the data module in the "second mode" must be:

> configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module.

Id. Independent Claim 19 includes similar requirements for the claimed "modes." *See id.* at cl. 19. There is no ambiguity to resolve as to what happens in the first mode and second mode in the claim.

The Samsung/Google proposed construction seeks to import the terms "normal" and "self-test" which are used in one embodiment in the specification. The specification makes clear that normal and test are two of the possible modes during which operations occur: "The memory subsystem [that] is operable in any of **a plurality of modes *including*** a normal mode and a test mode." Ex. 1 ('523 Patent) at 2:38-47. The Federal Circuit holds that the terms "plurality" and "including" are non-limiting. *See SIMO Holdings Inc. v. Hong Kong uCloudlink Network Tech. Ltd.*, 983 F.3d 1367, 1377 (Fed. Cir. 2021) ("The phrase 'a plurality of' means 'at least two of.'"); *Apple Inc. v. Voip-Pal.com, Inc.*, 976 F.3d 1316, 1323 (Fed. Cir. 2020) (citing *inter alia* Black's Law Dictionary (11th ed. 2019) ("The participle including typically indicates a partial list.")). The specification is clear that "test" and "normal" modes are only examples and that "normal" is only one example of a "non-test mode."

> **For example**, the memory module 10 may default to ***a non-test mode (e.g., normal operational mode)*** and the switches 44 of the data handlers 30 and the memory device controller 34 are not configured in a test mode. **For example**, configuring the test mode may include switching (e.g., by configuring the test controller 36) the

> mode of the memory module 10 from a normal operation mode to the test mode. Ex. 1 ('523 Patent) at 13:59-14:4.

Nothing in the specification supports, let alone requires, Samsung/Google's construction that the "first" mode must be a "normal" mode. *See, e.g.*, Ex. 1 ('523 Patent) at 15:9-12 ("For example, the testing logic (e.g., the control module 22 and/or the data module 28) may be generally inactive and the memory module 10 may default to a **functional** (e.g., non-test) mode."). Samsung/Google could just as arbitrarily proposed a "functional" mode as the first mode. There is also nothing in the specification indicating that the patentee intended to act as a lexicographer, so that one must impose a requirement that "second" can only mean "self-test." The above passages refer to an exemplary "test" mode, without using the additional modifier "self."

The prosecution history further supports Netlist's position that the normal and self-test are exemplary modes and that it is improper to read these limitations into the claims. In a February 8, 2018 Amendment, Netlist amended the claims to remove references to "normal mode" and "test mode" from the relevant claims.

> wherein the memory module is operable in any of a plurality of modes including a first mode and a second mode ~~normal mode and a test mode~~;

Ex. 8 (2018-02-08 Amendment) at 3. Netlist made this amendment to overcome a Section 112(b) rejection and emphasized that the nature of the "first mode" and "second mode" are expressly defined in the claim. *Id.* at 18-19. Netlist made the amendment removing the "test" and "normal" language in response to a December 18, 2017 Office Action indicating that the term "test mode" created confusion, not clarity, in the claim. Ex. 7 (2017-12-18 Office Action) at 5-7. Simply put, Samsung/Google want to add back into the claim two specific terms "normal" and "test" that were removed by Netlist from the claim, based on rejection by the examiner because of the presence of those terms.

2. Samsung and Google's Answering Position

The '523 patent states that the "*present invention*" relates to "*self-testing* electronic memory modules." '523 patent at 1:32–34 (emphasis added). To that end, the '523 patent consistently and exclusively describes embodiments of a self-testing memory module that operate in two modes: a "normal [non-test] mode" and a "self-test mode." While the two modes described in the '523 patent claims are a "first mode" and a "second mode," the intrinsic evidence—including the specification, prosecution history, and Netlist's statements in IPR proceedings—confirm that "first mode" and "second mode" mean "normal [non-test] mode" and "self-test mode," respectively.

a) "First Mode" and "Second Mode" Must Be Construed With Reference to the Specification

Per *Phillips,* "the specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Phillips v. AWH,* 415 F.3d 1303, 1315 (Fed. Cir. 2005) (cleaned up). Here, the specification consistently and exclusively describes that the "first mode" is the "normal" mode and the "second mode" is the "self-test" mode. '523 patent at 3:32–16:52.

While the "Abstract" of the '523 patent and the "Summary of the Invention" state that the purported inventive memory module "is operable in any of a plurality of modes including a normal mode and a test mode," the specification only identifies and describes a "normal mode" and a "test mode." '523 patent, Abstract, 2:33–3:6. Notably, a "normal mode" or "normal operational mode" is described or referenced five times[5] and a "test mode" or "self-test mode" is described or referenced 25 times. No other modes are identified in the specification, much

[5] The specification repeatedly notes that the "normal mode" is the "non-test" mode, and one time also calls it the "functional (e.g., non-test) mode." '523 patent at 15:12.

less described. Since no modes other than "normal mode" and "test/self-test mode" are taught by the specification, the claimed "first mode" and "second mode" must be construed to mean, respectively, "normal [non-test] mode" and "self-test mode."

Netlist's own statements during IPR proceedings confirm that Samsung and Google's proposed construction is correct:

> The '523 Patent's ***first mode of operation is a normal mode (sometimes referred to as the "non-test mode")*** in which the data module propagates data signals between the system memory controller and the memory devices. The ***second mode of operation is a self-test mode*** in which the data module isolates the memory devices from being accessed by the system memory controller while it sends data patterns to the memory devices.

Ex. 20 (IPR2022-00063, POPR) at 3 (cleaned up, emphases added); *accord* Ex. 21 (IPR2020-01421, POPR) at 14–15. Netlist's expert, Dr. Brogioli, similarly opined that "a POSITA would understand that ***the claims of the '523 Patent*** are directed to a memory module that has been implemented into a host system and ***all require the claimed memory modules to function . . . [in] a second (test) mode*** (where signals are generated by the module itself)." Ex. 23 [Aug. 4, 2022 Decl. of Michael C. Brogioli, Ph.D. in Support of POR] ¶ 73. Accordingly, the two modes are "normal (non-test) mode" and "self-test mode." *See Aylus Networks, Inc. v. Apple Inc.,* 856 F.3d 1353, 1360–61 (Fed. Cir. 2017) (holding that patent owner's statements in IPRs may be used to construe and limit scope of claims under doctrine of prosecution disclaimer).

The Federal Circuit has routinely held that claims cannot enlarge what is patented beyond what the inventor described as her invention. When the specification "consistently" and "exclusively" describes an element in a certain manner in various embodiments, that is "clearly" what the inventor invented, and informs (and limits) the proper construction of such elements. *See, e.g.*, *GPNE Corp. v. Apple Inc.*, 830 F.3d 1365, 1370–71 (Fed. Cir. 2016) (holding that district court did not err in characterizing a "node" as a "pager" where specification consistently

and exclusively described invention as a system of pagers); *Eon Corp. IP Holdings v. Silver Spring Networks*, 815 F.3d 1314, 1320–23 (Fed. Cir. 2016) (holding that although terms "portable" and "mobile" might theoretically, in the abstract, be interpreted broadly as anything that is capable of being moved, specification's extensive discussion and use of terms mandates constructions that are tethered to patent's description of the invention); *Nystrom*, 424 F.3d at 1144–45 (construing "board" to mean "wood cut from a log" in light of specification's consistent use of term, because patentee "is not entitled to a claim construction divorced from the context of the written description and prosecution history").

Like the cases above, a review of the '523 patent specification leads to the inescapable conclusion that the terms "first mode" and "second mode" have a meaning within the context of the specification that is *not as broad* as the ordinary meaning divorced from the patent's disclosure.

b) The Prosecution History Confirms that the Claims are Directed to "Normal" and "Self-Test" Modes

Netlist's amendments during prosecution make clear that "first mode" and "second mode" mean "normal [non-test] mode" and "self-test mode," respectively. Netlist originally sought claims explicitly requiring a "normal mode" and a "test mode," rather than a "first mode" and a "second mode." Ex. 3 ['523 FH, Mar. 29, 2014 Application] at 25–28. Nearly four years later, Netlist *sua sponte* amended the pending claims to replace "normal mode" with "first mode" and "test mode" with "second mode." Ex. 8 ['523 FH, Feb. 8, 2018 Amendment] at 3–11. Netlist explained to the examiner that this amendment was made simply "to *rename* some of the claim terms" and "no new matter is added." *Id.* at 12 (emphasis added). Accordingly, by Netlist's own admission, the "renam[ing]" of the claim terms did not broaden or significantly alter the scope of the then-pending claims.

Netlist argues that it made this amendment removing the "test" and "normal" language in response to a Section 112(b) rejection, *supra* at 19, but that is incorrect. First, the Section 112(b) rejection did not concern the "normal mode" at all. Ex. 7 ['523 FH, Dec. 8, 2017 Office Action] at 4–6. Second, the examiner did not state that the term "test mode" required clarification; instead, the examiner sought clarification concerning the manner in which the "self-test data patterns," recited elsewhere in the then-pending claim, perform a test of the memory devices. *Id*. In response, the applicant attempted to traverse the rejection through argument that only highlights the importance of construing "second mode" as "test mode"—the applicant emphasized the claim's focus on testing:

> It is within the knowledge of those skilled in the art that memory modules are commonly tested by transmitting test data to their memory devices, which can be configured to receive and store the test data according to address and control signals. The test data are then read back from the memory devices for comparison. See, for example, US6829728B2 and US6928593B1, which are cited in the Information Disclosure Statements filed on February 15, 2016 in the present application.

Ex. 8 ['523 FH, Feb. 8, 2018 Amendment] at 18. Third, the applicants specifically told the examiner that the amendment was just a "renam[ing]."

Netlist's litigation-driven claim construction is at odds with the prosecution history and contrary to law. Where an amendment broadens a claim beyond the subject matter disclosed in the written description as originally filed, the claim should be construed narrowly and limited to what is supported by the written description. *See, e.g.*, *Schering Corp. v. Amgen Inc.*, 222 F.3d 1347, 1354 (Fed. Cir. 2000) (substituted claim term construed only as consistent with scope of original term used at filing, and not the broader meaning, to avoid new matter concerns because "to grant broader coverage would reward [the inventor] for inventions he did not make"). As described above, the terms "first mode" and "second mode" do not appear anywhere in the specification of

the '523 patent. Instead, the specification consistently and exclusively describes a "self-testing memory module" that operates in a "normal mode" and a "test mode."

c) The Court Should Reject Netlist's Proposed Construction Because It Improperly Seeks to Enlarge What Is Patented

Netlist argues that no construction is necessary for these terms. According to Netlist, the plain language of the claims describes "what happens" in the "first mode" and "second mode."[6] *Supra* at 17–18. Netlist does not dispute, however, that "what happens" in the two modes *mirrors exactly* the specification's description of the "self-testing memory module" that operates in a "normal mode" and a "test mode." Netlist argues against Samsung and Google's proposed construction on the ground that the specification occasionally uses "non-limiting" language, *e.g.*, "a plurality of modes *including* a normal mode and a test mode"; "[f]or example, the memory module 10 may default to a *non-test mode (e.g., normal operational mode*). *Supra* at 18–19. But such non-limiting language, by itself, cannot justify expanding the scope of the claims beyond what the inventors described as their invention as a matter of law.

Rather, Federal Circuit law is clear that a patent holder cannot escape having the invention's scope limited to what is actually described in the patent merely by incorporating non-limiting language throughout the specification. For example, in *Bell Atlantic Network Servs., Inc. v. Covad Comm. Group, Inc.,* 262 F.3d 1258, 1269–75 (Fed. Cir. 2001), the Federal Circuit determined the proper construction of the term "plurality of different modes." The patentee argued the "ordinary meaning of the word 'mode,'" is broad and could encompass many modes, not just the three modes specifically disclosed in the specification. The Federal Circuit disagreed: "the ordinary meaning of the non-technical term 'mode' is sufficiently broad and

[6] In an earlier case involving the '523 patent, Netlist asserted that the specification "compels" the conclusion that "mode" means a "distinct behavioral state that a system may be switched to." Ex. 16 [20-cv-00194-ADA, D.I. 80 (W.D. Texas)] at 6.

amorphous that the scope of the claim language can be reconciled *only with recourse to the written description*." *Id.* at 1269–70 (emphasis added). The Federal Circuit concluded the specification consistently used the term "mode" to refer to three specifically-disclosed "modes." Even though those modes were labeled "preferred" embodiments and the specification also broadly and generically disclosed "a plurality of different modes," the Federal Circuit held that "the three modes described in the Detailed Description of the Preferred Embodiments describe the three possible modes of the invention, *and the claims are not entitled to any broader scope.*" *Id.* at 1270–73 (emphasis added).

Similarly, in *Medicines Co. v. Mylan, Inc.,* 853 F.3d 1296, 1307–09 (Fed. Cir. 2017), the Federal Circuit determined the meaning of the term "efficient mixing" in a patent that included a "detailed description [that] provide[d] a laundry list of mixing techniques that individually (or in combination) may (or may not) constitute efficient mixing." Rather than hold that anything the specification identified as possibly constituting "efficient mixing" was within the scope of the term, the Federal Circuit looked to the lone example of "efficient mixing" and limited the term to that example, even though that example was explicitly identified as "non-limiting." *Id.* at 1309. The Federal Circuit did so because that example was:

> the only description of efficient mixing in the patents in suit that casts light on what efficient mixing is and that enables one of ordinary skill in the art to achieve the objects of the claimed invention . . . . No other part of the patents' written description ***sufficiently teaches the affirmative steps*** that constitute efficient mixing. In this circumstance, we think it entirely appropriate to limit the term "efficiently mixing" to the sole portion of the specification that adequately discloses "efficient mixing" to the public.

Id. (emphasis added). The court thus chose the "non-limiting" example's specific meaning over the "detailed description's open-ended and vague teachings," as "necessary to 'tether the claims to what the specification[] indicate[s] the inventor actually invented.'" *Id.*

3. Netlist's Reply Position

Defendants do not dispute that the claims already define what the first and second modes entail:

> wherein the control module in the ***first mode*** is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals; and
>
> wherein the control module in the ***second mode*** is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module.

Thus, as Netlist stated during prosecution, replacing "normal mode" with "first mode" and "test mode" with "second mode" involved only "renam[ing] some of the claim terms" with "no new matter [] added." Ex. 8 at 12. This is because the meaning of the "first mode" and "second mode" is defined by the claim language in the element that follows the appearance of the terms "first mode" and "second mode." If the words "normal" and "test" mean something different from the claim language that follows the terms "first mode" and "second mode," Defendants had the opportunity in their brief to explain what that additional or different meaning is. Lurking behind Defendants' unwillingness to explain what "normal mode" and "test mode" add to "first mode" and "second mode" is the danger that their expert will later pour additional meaning into these terms, requiring a second round of claim construction. This is not proper. Claim construction is

the time for Defendants to explain how "test" and "normal" add meaning beyond the claim language that replaced these terms during prosecution.

The portions of the specification cited by Defendants make clear that the label used to describe a given mode is not meaningful. *Supra* at 20–21. The specification uses the terms "normal mode," "normal operational mode," "functional mode," or "non-test mode" when describing a first mode. *See, e.g.*, '523, 2:40, 13:60, 15:12. The specification uses the term "test mode" or "self-test mode" when describing a second mode. *See, e.g.*, '523, 2:45, 15:14.

Bell Atlantic is distinguishable because there the patentee attempted to construe "mode" in a manner directly contradicted by the specification and prosecution history. *See Bell Atl. Network Servs., Inc. v. Covad Commc'ns Grp., Inc.*, 262 F.3d 1258, 1269-75 (Fed. Cir. 2001). Specifically, the patentee's desired construction would allow additional modes based on changes in "rate of data transfer (as opposed to bandwidth)." *Id.* at 1269. That construction was contradicted by the specification's use of "the terms 'rate' and 'mode' to refer to separate and distinct concepts." *Id.* at 1270. The proposed construction was also inconsistent with the prosecution statement "that the 'mode' of the present invention varies solely by changing the amount of bandwidth allocated between the upstream and downstream channels." *Id.* at 1274. Here, in contrast, a plain and ordinary construction of the terms "first mode" and "second mode" would not contradict anything in the specification or prosecution history and instead gives primacy to the claim language. *Medicines Co.* is equally distinguishable. *See Medicines Co. v. Mylan, Inc.*, 853 F.3d 1296 (Fed. Cir. 2017). There, the patentee attempted to construe the term "efficient mixing" expansively, and the court limited it to "Example 5" of the specification, the only description of efficient mixing in the specification. *See id.* at 1307-09. Additionally, "Medicines relied on the mixing parameters of Example 5 to overcome prior art cited during prosecution and did not cite any other examples of

efficient mixing." *Id.* at 1308. Here, there is no similar undermining statements during prosecution. Additionally, the actual structures and operations of the claimed "first" and "second mode" are fully disclosed in the claim limitation. A plain and ordinary construction would not result in claims that are unmoored from the specification, as was the concern in *Medicines Co*. *See id.* at 1307-09.

Defendants dispute whether Netlist replaced "normal mode" and "test mode" with "first mode" and "second mode," respectively, in response to a 112 rejection. *Supra* at 22-23. But the file history confirms that the amendment was precipitated by a 112 rejection:

Rejection of Claims 1-5, 7-8, 10-12, 26-29 and 36 under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), Second paragraph

The Office Action rejected claim 1 under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, citing line 19-29 of claim 1 and stating:

> "[It] is not clear whether, during the test mode, the self-test data patterns that are received by at least a portion of the memory devices according to the self-test address and control signals from the control module is actually doing the test for that the at least a portion of the memory devices according to the self-test address and control signals from the control module or just for storage over there? How the at least a portion of the memory device is tested is unclear and what is the result and/or what to with the test result?"

Ex. 8 at 18. In response to this rejection, the inventors amended the claims and spoke instead about a "first mode" and "second mode" and explained how the language that follows these terms defines the operation in a way to overcome the Section 112 rejection.

Claim 1 recites a memory module that improves upon the prior art by being operable in any of a plurality of modes including a first mode and a second mode, and by including, among other things, a control module and a data module configured to perform certain functions depending on whether the memory module is in the first mode or second mode. For example, the data module in the first mode "is configured to propagate first data signals between the memory devices and the system memory controller", and in the second mode is configured "to isolate the memory devices from being accessed by the

> system memory controller and to transmit second data signals having data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module." These limitations are consistent with the teachings of the Specification. (See, for example, paragraphs [0025]-[0026] and [0041]-[0042]).

Id. at 18-19. The prosecution history emphasizes that the terms "normal" and "test" were replaced with "first" and "second" mode because the element in which the term appears defines the mode.

Defendants' discussion of Netlist and Dr. Brogioli's statements at IPR is a misdirection. When the term "normal" or "test" is used in these statements, it has the meaning expressed in the claim language that defines "first mode" and "second mode." *See, e.g.*, Ex. 20 (IPR2022-00063, POPR) at 3; Ex. 23 (2022-08-04 Decl. of Michael C. Brogioli) ¶¶ 49, 73. The pernicious issue in this proceeding is that Defendants can wait to disclose what they think "normal" and "test" means and how this is different from the claim element definition.

4. Samsung and Google's Sur-Reply Position

Netlist admits that in the recent IPR involving the '523 patent, Netlist and its experts repeatedly characterized ***the claims*** in the '523 patent as reciting a "normal" mode and a "test" mode. *Supra* at 29; *see also* Ex. 26 (IPR2022-00063, Brogioli Tr.) at 194:5–14 ("Q: Test mode is the second mode in the claims, right? A: In the claims, correct. … Q: And is it fair to characterize the first mode of the claims as normal mode? A: I think I use that phrase myself, yes."); Ex. 22 [IPR2022-00063, Brogioli Decl. in Support of POPR] ¶ 26.

Netlist concedes that the amendment during prosecution that replaced "normal mode" and "test mode" with "first mode" and "second mode" involved only "renam[ing] some of the claim terms" with "no new matter [] added." *Supra* at 26. In spite of this admission, Netlist rejects Samsung and Google's proposed construction—presumably because Netlist intends to read the claims more broadly, to cover something *other than* "normal" or "test" modes. Netlist's proposal

contravenes Federal Circuit precedent holding that claims cannot enlarge what is patented beyond what the specification "consistently" and "exclusively" describes as the invention. *Supra* at 21–22 (citing *GPNE Corp.*, *Eon Corp.*, *Nystrom*). Netlist's reply does not address this case law.[7]

With respect to Samsung and Google's cited case law that Netlist does address, Netlist fails to engage on the relevant portions of the opinions. Samsung and Google discussed the *Bell Atlantic* and *Medicines Co.* opinions to establish that a patentee cannot expand the invention's scope beyond what is described in the patent by incorporating non-limiting language throughout the specification. *Supra* at 24–25. Netlist does not dispute this basic point. Netlist argues that *Bell Atlantic* and *Medicines Co*. are distinguishable because the patent holders in those cases sought constructions in litigation that were inconsistent with statements made during prosecution, but that is precisely what Netlist is doing. Netlist made statements in IPRs that contradict Netlist's current interpretation of "first mode" and "second mode," and those statements are disclaimers as a matter of law. *See Aylus Networks, Inc. v. Apple Inc*, 856 F.3d 1353, 1360–61 (Fed. Cir. 2017).

Finally, Netlist says Samsung and Google dispute that Netlist's amendment replaced "normal" and "test" with "first" and "second" "in response to a 112 rejection." *Supra* at 28. While the amendment did occur after the 112 rejection, nothing Netlist points to shows it was in "response" to a 112 rejection. Indeed, the examiner did not state that "normal mode" or "test mode" required clarification, and Netlist did not argue that "renam[ing]" the modes resolved the 112 rejection. Thus, the premise of Netlist's argument that the amendment was made "because the element in which the term appears defines the mode," *supra* at 29, is demonstrably false.

[7] Netlist argues that the "label" used to describe a given mode is "not meaningful," *supra* at 27, but Netlist's opposition to Samsung and Google's proposed construction demonstrates otherwise. Further, even Netlist agrees that the specification repeatedly uses the terms "test" and "self-test" interchangeably to describe the "second mode." *Id*.

C. "data module" (cls. 1, 2, 6, 7, 15, 18)

Samsung & Google's Proposed Construction	Netlist's Proposed Construction
"integrated circuit package including at least one data handler"[8]	"circuitry that can enable data paths between a memory device and a system memory controller in one mode and can isolate memory devices from the system memory controller in another mode"

1. Netlist's Opening Position

The "Abstract" and "Summary" both make clear what a data module is: "the data module enables data paths between the memory devices and the system memory controller"; "the data module isolates the memory devices from the system memory controller." Ex. 1 ('523 Patent) at Abstract, 2:32-47. The Samsung/Google construction imports two limitations found nowhere in the specification and excludes all of the major embodiments in the specification. First, nothing in the specification requires the data module be an IC package; second, nothing in the specification requires multiple data handlers.

First, the specification teaches that a given data module may only have one data handler, which is less than a plurality: "In certain embodiments, the data module 28 comprises a plurality of data handlers 30. In other embodiments the data module 28 includes at least one data handler 30." *Id.* at 10:7-13. Although a given claim may place additional limitations on the number of data handlers, nothing in the specification necessarily requires multiple data handlers.

Second, when a data module has a plurality of data handlers, each data handler can be present in separate physical packages:

> In certain embodiments, the plurality of data handlers 28 comprises at least two physically separate components mounted on the PCB 12. For example, the plurality of data handlers 28 may include at least two physically separate integrated circuit

[8] Samsung and Google have revised their proposed construction to reflect "at least one" data handler, rather than "a plurality of" data handlers, to narrow the issues and render moot certain criticisms raised in Netlist's opening brief. *See, e.g.*, *infra* at 31.

> packages. The physically separate integrated circuit packages are mounted on different portions of the PCB 12 in some embodiments. *Id.* at 9:10-16.

Consistent with this disclosure, Figures 1-3 depict the data handlers 30 in independent, bold line boxes (highlighted below in blue), with the "data module" being the collective operation of all of the data handlers as depicted by the dashed line box (highlighted below in red). This is not an accident. The specification is clear that the various functional units can comprise "discrete" components and "one or more" processors:

> In various embodiments, the components of the data module 28 (e.g., the switch 44, the data handlers 30, the data handler logic element 46, the data generation element 54, and/or verification element 56) may include discrete logic, one or more application-specific integrated circuits (ASICs) one or more microprocessors, one or more field-programmable gate arrays (FPGAs), or one or more computer programmable logic devices (CPLDs). *Id.* at 12:43-50.

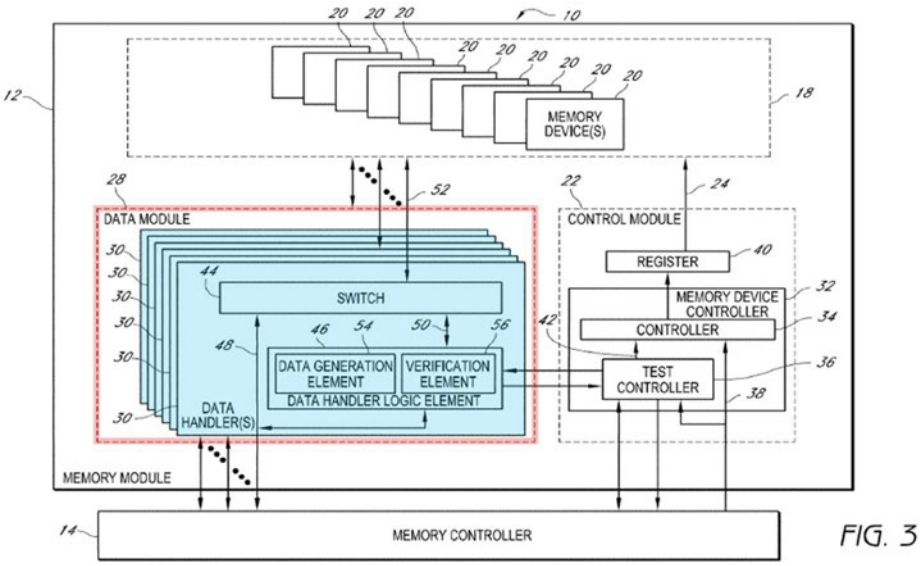


FIG. 3

Third, in the specification, "modules" need not be single integrated circuit packages—they are collections of devices. Figures 1-3 depict a "memory module" which comprises a "data module" and a "control module." The "module[s]" are not necessarily single integrated circuit packages, as evidenced by the fact that each module is itself composed of discrete components, such as "memory devices," "data handers," "registers," and "memory device controller."

In the PTAB, Samsung proposed a plain and ordinary meaning construction of the term. Ex. 19 (Petition, IPR2022-00063) at 15. The PTAB did not add the extraneous limitations Samsung is currently advancing. *See* Ex. 28 (FWD, IPR2022-00063) at 11-12.

2. Samsung and Google's Answering Position

Claim 1 of the '523 patent recites a "memory module" comprising "memory devices mounted on a circuit board," "a ***data module*** mounted on the circuit board," and "a control module mounted on a circuit board" (emphasis added). The specification describes an embodiment of the "data module" as "compris[ing] one physical component," as opposed to a module made up of disparate components. '523 patent at 12:60–62.

To be "mounted on [a] circuit board," the data module of claim 1 must be a packaged integrated circuit. Indeed, this is what Netlist said during prosecution. Netlist distinguished Zuraski by arguing that Zuraski fails to disclose the "memory module" of claim 1 because, among other things, Zuraski's embedded components "do not include the mechanisms (e.g., the input/output circuits and proper packaging) for mounting on a circuit board." Ex. 5 ['523 FH, July 11, 2016 Applicant Response] at 17–18. Through this statement, Netlist acknowledged that only packaged integrated circuits include the mechanisms for mounting on a circuit board. Accordingly, Samsung and Google's proposed construction, which defines the "data module" as "an integrated circuit package," is correct.

Netlist argues that the specification teaches that "modules" "need not be single integrated circuit packages," and each "module" may itself include additional discrete components. *Supra* at 31–32. But this argument misses the point and ignores the claim language. Claim 1 specifies that it is ***the "data module"*** that is mounted to the circuit board. Samsung and Google's proposed construction does not prevent the packaged "data module" from including other components. The portions of the specification on which Netlist relies are more aptly applied to claim 19, which

specifies *components* that are separately packaged. *See* '523 patent, Claim 19 ("a plurality of data handlers mounted on the PCB"); *see also id*. at 12:56–60 ("[I]n one embodiment, each of the data handlers 30 and the corresponding switch 44, data generation element 54, and verification element 56 comprise one physical component (e.g., are included in one integrated circuit package).)"

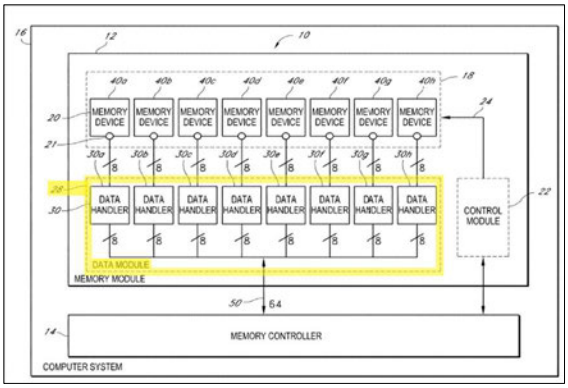
3. Netlist's Reply Position

Defendants attempt to limit "data module" to a single "integrated circuit package …." Defendants support their proposed construction by pointing to "an embodiment" where data module "comprises one physical component." *Supra* at 33. But the '523 patent includes many other embodiments where the data module comprises multiple integrated circuit ("IC") packages. *See supra* at 31-32 (citing *inter alia* '523, Figs. 1-3). A construction, like that by Defendants, that excludes preferred embodiments is "rarely if ever correct." *Kaufman v. Microsoft Corp.*, 34 F.4th 1360, 1372 (Fed. Cir. 2022).

Defendants argue that the "mounting" requirement in independent claim 1 requires a single IC package. *Supra* at 33. But the specification describes embodiments in which the data module comprises multiple separate components that are "mounted." For instance, Figure 2 labels the plurality of data handlers 28 as the "data module," and the specification describes how it may comprise "physically separate integrated circuit packages mounted on different portions of the PCB 12":

In certain embodiments, the plurality of data handlers **28** comprises at least two physically separate components mounted on the PCB **12**. For example, the plurality of data handlers **28** may include at least two physically separate integrated circuit packages. The physically separate integrated circuit packages are mounted on different portions of the PCB **12** in some embodiments. For example, each of the eight data handlers **30***a*-**30***h* shown in FIG. **2** may include physically separate integrated circuit packages mounted on different portions of the PCB **12**. While eight data handlers **30** are shown in FIG. **2**, other numbers of data handlers **30** are possible including fewer or more than eight.

'523, 9:12-16.



'523, Fig 2.

Defendants argue that claim 19 covers the embodiment in which the data module comprises multiple integrated circuits. *Supra* at 33–34. Claim 19 recites "a plurality of data handlers mounted on the PCB." This language makes clear that multiple separately packaged components that operate together can be mounted on a PCB. Furthermore, claim 1 recites "***a*** data module." "[A]" in claim language means one or more. *See FS.com Inc. v. Int'l Trade Comm'n*, 65 F.4th 1373, 1377 (Fed. Cir. 2023). Therefore, claim 1, like claim 19, covers embodiments in which there are multiple separately packaged data handler components mounted because the specification describes a data module as comprising multiple data handler components.

Defendants argue that Netlist's prosecution statement limits "data module" to a single physical component. *Supra* at 33. But the statements it points to relate to "memory module," not "data module." Indeed, the specific statement quoted by Defendants (red text below) relates to Zuraski's "embedded memory units 16a-b" and has nothing to do with the data module:

> … ***Zuraski does not even disclose a memory module***. A memory module is a printed circuit board on which memory integrated circuits (memory devices) are mounted (http://en.wikipedia.org/wiki/Memory_module; also, Specification paragraph [0024] and FIG 1). Zuraski, on the other hand, is all about a microprocessor 10, which is not a memory module. A microprocessor is a computer processor which incorporates the functions of a computer's central processing unit (CPU) on a single integrated circuit (IC) . . . . **As such, the microprocessor 10 in Zuraski has embedded memory units 16a-16b** (Zuraski, FIG. 1, and col. 5, line 50, emphasis added). **These embedded memory**

> **units 16a-b are memory cells embedded in the microprocessor integrated circuit** (Zuraski, col. 6, lines 48-52) **and do not include the mechanisms (e.g., the input/output circuits and proper packaging) for mounting on a circuit board** (Zuraski, col. 6, lines 48-64). . . .

Ex. 5 at 18-19 (emphasis added).

Defendants' proposed construction is also inconsistent with the positions Samsung took in IPR2022-00063, which challenged the '523 patent. There, Samsung mapped the claimed "data module" to "nine switch ASICs ("D")," i.e., multiple integrated circuit packages, instead of the single IC package it now proposes.

c) [1.c] Data Module

In Ellsberry's First and Second Embodiments, the nine Switch ASICs ("D") in FIGS. 5-6 collectively comprise "*a data module*," EX1003,¶186, correspond to Switch ASICs 206-208 (FIG. 2), *id.*; EX1005,¶¶[0049],[0051], and pass data between the memory devices and the memory bus/memory controller. EX1003,¶186; EX1005,¶¶[0028-0030].

Ellsberry discloses the Switch ASICs are "*mounted on the circuit board*" in FIGS. 5-6. EX1003,¶187; EX1005,¶¶[0003],[0047].

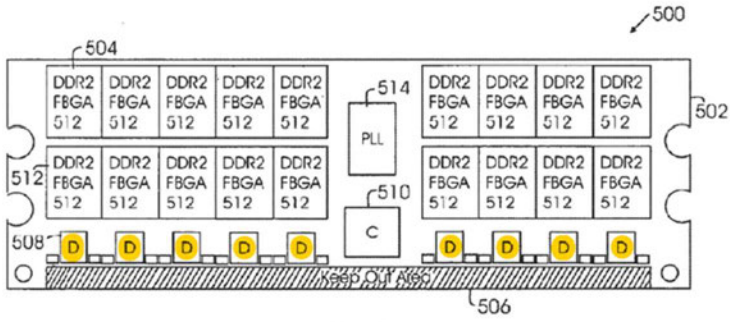


Fig. 5

Ex. 19 at 40-41. It is axiomatic that claims are to be construed consistently for infringement and validity. *TVIIM, LLC v. McAfee, Inc.*, 851 F.3d 1356, 1362 (Fed. Cir. 2017).

4. Samsung and Google's Sur-Reply Position

Netlist's primary argument in reply is that Samsung and Google's construction would

exclude "preferred" embodiments. As an initial matter, the '523 patent does not label any embodiment as "preferred." In any event, applicants are not required to focus their claims on a preferred embodiment; they are free to claim any alternative embodiments described in the specification. *See Helmsderfer v. Bobrick Washroom Equip., Inc.*, 527 F.3d 1379, 1383 (Fed. Cir. 2008) ("It is often the case that different claims are directed to and cover different disclosed embodiments. The patentee chooses the language and accordingly the scope of his claims."). Here, Netlist admits that the specification describes an embodiment wherein the data module "comprises one physical component," '523 patent at 12:60–62, which is consistent with claim 1's requirement that the "data module" itself is mounted to a PCB.

Netlist also does not dispute that during prosecution the applicant told the Patent Office that only packaged integrated circuits include mechanisms permitting mounting on a circuit board. The fact that this statement was made while discussing the term "memory module," rather than the term "data module," is irrelevant. What matters is that Netlist took a position on what is required for a component to be "mounted on a circuit board"—and it is undisputed that claim 1 recites a "data module mounted on the circuit board . . . ." '523 patent at 16:60.

Finally, the proper construction of "data module" was not determined in the recent IPR, where Netlist took the position that the term's construction "do[es] not bear on the issues in dispute." Ex. 28 [IPR2022-00063 FWD] at 11. The construction did not matter because one of the two references (Jeddeloh) disclosed a "data module" with a single package. Ex. 27 [IPR2022-00063, Petitioner's Demonstratives] at 12.

D. "data handler logic element[s]" (cls. 1, 2, 5, 10, 14, 17, 19, 23)

Samsung & Google's Proposed Construction	Netlist's Proposed Construction
"circuitry within the data handler that generates the data patterns"	"one or more discrete circuits, application specific integrated circuits, field programmable gate arrays, or

	computer programmable logic devices that can read and/or write data from less than all of the data ports on the memory devices on the module without being in communication with other data handler logic elements"

1. Netlist's Opening Position

The claim language specifies that "the data handler logic element" "provide[s]" data patterns": "data patterns ***provided by the data handler*** logic elements to the data ports of the memory devices according to one or more commands output from the control module." Samsung/Google's proposed construction re-writes the claim, replacing "provides" with "generate." The specification speaks of the data module "generat[ing]" data patterns in certain embodiments.

> As described more fully below, **in certain embodiments the data module 28 generates test data patterns** to write to the plurality of memory devices 18 of the memory module 12 and checks the data patterns read or received back from the plurality of memory devices 18 for agreement with corresponding data patterns that are expected to be read back from the plurality of memory devices 18. Ex. 1 at 5:28-33.

If it were proper to limit the claim to a single embodiment—it is not—this would counsel in favor of the *data module* requiring generation of data patterns, not the data handler logic. Samsung/Google do not propose adding a generation limitation to the construction of "data module." Instead, within the optional embodiment in which the data module generates test pattern data, there is another optional sub-embodiment in which the data handler logic circuit can generate the data patterns:

> Each of the data handlers 30 of certain embodiments further includes a data handler logic element 46. ***The data handler logic element 46 of certain embodiments comprises a data generation element*** 54 and a verification element 56. The data generation element 54 ***may be configured to generate data signals (e.g., patterns of data signals)*** for writing to the corresponding plurality of data ports, for example. The data signals and/or patterns of data signals may be based on information (e.g., programming or configuration information) the data handler logic element 46 receives from the control module 22, for example. *Id.* at 10:37-47.

This embodiment can be contrasted with earlier discussions of the data handler logic circuit in which instead of "generat[ing]" the data signals, the specification only teaches that the data signals are "from" the data handler logic element:

> "data signals 50 ***from*** the data handler logic element 46." *Id.* at 10:20-21.
>
> "inputs the data signals 50 ***from*** the data handler logic element 46 during a test mode." *Id.* at 10:3-31

Ultimately, Samsung/Google are seeking to re-draft the claim by replacing the term "provide" with "generate," ignoring the embodiment that involves data patterns being "from" the data handler logic circuit. The problem is that this simply creates another fight about what the word "generate" means. For example, based on the parties' June 30, 2023, meet and confer, Samsung/Google apparently plan to argue that when a data handler bases data patterns "on information (e.g., programming or configuration information)" "receive[d]" from another source, this does not constitute "generate." The specification expressly describes basing data patterns on information received from another source as an example of generation at 10:44-47 ("The data signals and/or patterns of data signals may be based on information (e.g., programming or configuration information) the data handler logic element 46 receives from the control module 22, for example."). As a result, if the Court determines to replace the word "provide" with "generate," Netlist requests construction of "generate" to make clear that "generate" encompasses the data handler logic basing the data patterns on information, including programming or configuration information, received from another component, as well as the data pattern being "from" the handler logic circuit.

In a PTAB proceeding involving a parent of the patent in suit, the PTAB construed "generate" as encompassing providing data patterns based on information supplied from another component, citing the identical language at 10:44-47.

> Having considered the ordinary meaning of the term "generate" in the context of both the claims and the '434 patent as a whole, we agree with Patent Owner that the broadest reasonable interpretation of the claim term "generate" is "produce," and that "generate" does not mean "cause" or "cause to produce." We interpret the claim language "address and control signals **generated** by the control module and the data generated by the plurality of data handlers" (claim 1), and the corresponding limitations in claims 20 and 29, as encompassing signals and data that originated in these modules, ***including by transformation or modification of information and/or data received from another component.*** See e.g. Ex. 1001, 10:33–37 ("The data signals and/or patterns of data signals may be based on information (e.g., programming or configuration information) the data handler logic element 46 receives from the control module 22." (emphasis added)); *id.* at 10:57–59 ("The data may be generated based [on] previously written data (e.g., inverting each of the bits of a previously written data word)" (emphasis added)). We do not interpret this language as encompassing signals and data received by the data and control modules from another component, and merely provided, propagated, sent, or input to memory devices, without transformation or modification by the data and control modules. Ex. 29 (Final Written Decision, IPR2014-00970) at 32.

Although the PTAB applied the BRI standard of construction, because its construction was based on the express statements in the specification, the same result holds under *Phillips*. *See Kaufman v. Microsoft Corp.*, 34 F.4th 1360, 1372 (Fed. Cir. 2022) ("A claim construction that excludes a preferred embodiment is rarely, if ever correct and would require highly persuasive evidentiary support.").

The '523 patent was previously construed by Judge Albright in the Western District of Texas in a case involving SK Hynix. Counsel for Samsung represented SK Hynix. Judge Albright construed "data handler logic" as plain and ordinary meaning and data handler as "circuity for generating and processing data." Ex. 17 (*Netlist, Inc. v. SK Hynix Inc., et al.*, 6-20-CV-00194, 6-20-CV-00525, Dkt. 100 (Claim Construction Order)) at 4. His order contains no reasoning. He did, however, decline to adopt SK Hynix's construction on "generate," which was "circuit which generates and manages data," in which "generate means to produce (i.e., bring into existence, including by transformation and/or data received from another component), which does not include unpacking and packing data from a packet." *Id*. Because SK Hynix settled shortly after the issuance

of the construction, the Court did not engage the meaning of generate. Netlist acknowledges that the absence of reasoning makes Judge Albright's decision not to adopt SK Hynix's definition of generate of limited assistance to the Court.

In the PTAB, Samsung attempted to alter Judge Albright's construction, arguing that "a Skilled Artisan would understand the term 'generate' to mean 'produce (*i.e.*, bring into existence).'" Ex. 19 (Petition, IPR2022-00063) at 14. The PTAB declined to adopt this construction. *See* Ex. 28 (FWD, IPR2022-00063) at 11-12. Samsung/Google fails to acknowledge the planned gloss it will put on "generate" via expert testimony in front of the jury. There is clearly a dispute on this issue that is properly resolved at claim construction if the Court chooses to import a generate limitation into the claim.

The function performed by the data handler logic circuit is already described in the claims. Samsung/Google simply want, at best, to create ambiguity by replacing the word "provide" with "generate." Because the function is clear, if construction is to occur, that construction should describe the structure of the data handler logic circuit. 12:43-62 describes the structure of the components of the data module, including the data handler. Netlist's construction tracks this description. Moreover, this description is not limited to a single embodiment but describes all of the "various embodiments":

> In various embodiments, the components of the data module 28 (e.g., the switch 44, the data handlers 30, the data handler logic element 46, the data generation element 54, and/or verification element 56) may include discrete logic, one or more application-specific integrated circuits (ASICs) one or more microprocessors, one or more field-programmable gate arrays (FPGAs), or one or more computer programmable logic devices (CPLDs). . . . Ex. 1 ('523 Patent) 12:43-53.

In addition, the specification describes the structures that allow the data handler to perform its functions:

> Each data handler 30 is operable independently from each of the other data handlers 30 of the plurality of data handlers 28. For example, **each data handler 30 is**

> **configured to write to and/or read from the corresponding plurality of data ports of one or more of the memory devices 20 without being in communication any of the other data handlers 30 or other data ports of the memory devices** 20. *Id.* at 8:10-16.

Netlist's construction recites these same structures.

2. Samsung and Google's Answering Position

Netlist's argument for its construction oddly mirrors the process for construing a term under 35 U.S.C. § 112 ¶ 6. But this claim limitation does not recite any "means for" or similar language or otherwise dictate an application of § 112 ¶ 6. Netlist first argues that the function of the "data handler logic elements" is found in the claims. According to Netlist, this means that "data handler logic elements" should be construed to be the disclosed structure. Netlist then argues this structure is found in the '523 patent at 12:43–62. Contrary to Netlist's argument, this passage merely describes a number of generic implementation technologies that might be used to implement the "components of the data module" in "various embodiments." *Id.* Netlist's proposed construction fails to provide any guidance as to the meaning of "data handler logic elements," and omits the central feature set out by both the intrinsic and extrinsic evidence—that it generates data.

During prosecution, Netlist responded to a rejection under 35 U.S.C. § 101 by arguing, in part, that the Examiner "err[ed] by stating that the recited . . . 'data handler logic elements' . . . are well-known and conventional/generic computer components performing well-known and conventional/generic computer functions." Ex. 8 ['523 FH, Feb. 8, 2018 Amendment] at 17. According to Netlist, at the time the '523 patent was filed, "there were no well-known and conventional/generic" "data module[s]," and that the same applies to the other components of the claimed memory module. *Id.* Thus, the question remains: what is a "data handler logic element" if it is not well-known and conventional? The intrinsic evidence is the best source for determining this meaning.

The intrinsic evidence supports Samsung and Google's construction of "data handler logic element[s]" to mean "circuitry within the data handler that generates the data patterns." The specification consistently describes the claimed "data handlers" and the incorporated "data handler logic elements" as generating data patterns. Figure 3 of the '523 patent depicts a data module that includes "data handlers 30." *Id*. at 9:32–34, 10:7–10. Each of the data handlers "further includes a data handler logic element 46." *Id*. at 10:37–44. The data handler logic element includes a "data generation element" and "verification element." *Id.* Contrary to Netlist's proposed construction, the "data generation element" and "verification element" are the disclosed structural elements within the data handler logic elements. These disclosed structures are consistent with the purported purpose of generating test data to self-test the memory module's memory devices. *See id*. at 5:23–25 ("Each data handler 30 is further configured to generate data for writing to the corresponding plurality of data ports."), 6:3–7 ("Moreover, in the test mode, each of the data handlers 30 write the data generated by the data handler 30 to the corresponding plurality of data ports by selectively inputting data signals to the data ports of the plurality of memory devices 18."), 8:41–42 ("Each data handler 30 is further configured to generate data for writing to the corresponding plurality of data ports."), 10:37–40 ("Each of the data handlers 30 of certain embodiments further includes a data handler logic element 46. The data handler logic element 46 of certain embodiments comprises a data generation element 54 and a verification element 56."), 13:10–11 ("The data handler 30 is configured to generate cyclic data for writing to the corresponding plurality of data ports.").

"Where, as here, a patent 'repeatedly and consistently' characterizes a claim term in a particular way, it is proper to construe the claim term in accordance with that characterization." *Wisconsin Alumni Rsch. Found. v. Apple Inc.*, 905 F.3d 1341, 1351 (Fed. Cir. 2018) (holding term

"prediction" must be capable of receiving updates based on reading "patent as a whole"); *see also Nystrom*, 424 F.3d at 1144–45 (construing "board" to mean "wood cut from a log" in light of specification's consistent use of term, because patentee "is not entitled to a claim construction divorced from the context of the written description and prosecution history"). The '523 patent's specification repeatedly and consistently describes the data handler logic elements as generating data patterns. Every discussion of data handler logic elements includes at least the data generation element. *See Medicines Co.*, 853 F.3d at 1309.

Samsung and Google's proposed construction is also consistent with Judge Albright's construction of "data handler" in prior litigation in the Western District of Texas between Netlist and SK hynix. Netlist concedes that Judge Albright construed "data handler" as "circuitry for generating and processing data." *Supra* at 40, Ex. 17. Samsung and Google's proposed construction of "data handler logic element[s]" is fully consistent with this construction because the data handler logic elements are the part of the data handler for generating the data patterns.

Samsung and Google's proposed construction is also consistent with the way Netlist and its expert witnesses have repeatedly described the data handler/data handler logic elements in relation to the '523 patent and related patents.[9] For instance, Netlist and its experts have stated that the "data handlers generate data to test the memory devices and can compare the responses from the memory devices." Ex. 15 [Mangione-Smith CDCA Decl.] ¶ 59; Ex. 30 [Mangione-Smith Opening 1023 Rpt.] ¶ 62; Ex. 31 [Murphy Rebuttal Rpt., 337-TA-1023.] ¶ 38; Ex. 32 [CX-0005C] at Q/A 86; *see also* Ex. 33 [Inv. No. 337-TA-1023, Netlist's Prehearing Br.] at 20 ("The Self-Test Patents disclose that the data handlers generate data to test the memory devices and can compare

[9] The so-called "Self-Test Patent" family of related patents include U.S. Patent No. 8,001,434 (the "'434 patent").

the responses from the memory devices."). Consistent with these statements, the data handler logic elements are the structures within the data handler that "generate" data. This is confirmed by other Netlist admissions:

- Netlist's expert, Dr. Mangione-Smith, stated that "the term 'generate' is used consistently in the specification and the claims with the notion of **producing data in the data handlers** of claim 1 of the '434 Patent." Ex. 39 [Mangione-Smith Rebuttal Rpt.] ¶ 25 (emphasis added).

- Netlist argued that "[t]he term **'generate' in the Self-Test Patents is an action performed by the claimed data handlers**." Ex. 34 [Netlist's Posthearing Brief, 337-TA-1023] at 20 (emphasis added).

- Netlist acknowledged that "[t]he specification is rife with other examples of the **data handlers generating data** based on input information." Ex. 34 [Netlist's Posthearing Brief, 337-TA-1023] at 21 (emphasis added).

- Netlist's expert, Dr. Murphy, stated that [redacted].'" Ex. 31 [Murphy Rebuttal Rept., 337-TA-1023] ¶ 72 ([redacted]).

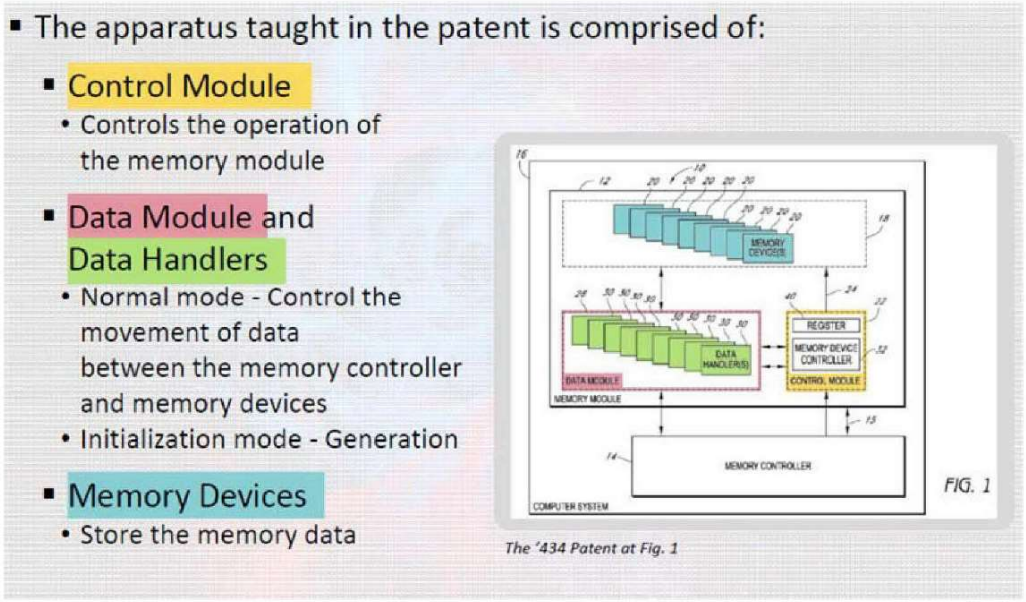
- Netlist argued that "[t]he proper and intended computing functionality of the intelligent logic resident in the [component of the accused product] (and the data handlers claimed in the Self-Test Patents) utilizes the information it receives (the Lego instruction manual) to operate on the data it receives (the required Lego pieces) **in order to generate a new data pattern**. Ex. 35 [Netlist Petition for Review] at 18 (emphasis added).

- Netlist and its expert, Dr. Brogioli, stated in its Patent Owner's Response that the "the **data module also generates data patterns** that are sent to memory devices while the control module generates the respective address and control signals needed for testing." Ex. 25 [IPR2022-00063, POR] at 13 (Aug. 4, 2022); Ex. 22 [Decl. of Michael C. Brogioli, Ph.D. in Support of POPR] ¶ 26 (Feb. 18, 2022); Ex. 23 [Decl. of Michael C. Brogioli, Ph.D. in Support of POR] ¶ 49 (Aug. 4, 2022); Ex. 11 [Brogioli Decl.,] ¶ 30 (emphasis added).

- Dr. Brogioli stated that "the **data handlers thereafter 'generate' said patterns** during a test." Ex. 23 [Decl. of Michael C. Brogioli, Ph.D. in Support of POR] ¶ 25 (emphasis added).

- Dr. Brogioli further explained that "a POSITA would understand that the claims of the '523 Patent are directed to a memory module that has been implemented into a host system and all require the claimed memory modules to function . . . [in] a second (test) mode (where **signals are generated by the module itself**)." Ex. 23 [Decl. of Michael C. Brogioli, Ph.D. in Support of POR] ¶ 73 (emphasis added).

Consistent with these statements, Netlist explained at the hearing in 337-TA-1023, with reference to the following slide depicting the "apparatus taught" in the specification, that the data handlers "control the movement of the data from the memory controller - to and from the memory controller and the memory devices" and "provide **generation of signals to help with the self-tests**." Ex. 36 [Inv. No. 337-TA-1023 Hearing Tr.] at 36–37 (emphasis added):



Notwithstanding the intrinsic evidence and all of these prior statements, Netlist criticizes Samsung and Google's construction as an attempt to "re-draft the claim by replacing the term 'provide' with 'generate.'" *Supra* at 39. Not so. First, Netlist's argument errs by conflating "provided" in surrounding claim language with the proper construction of the term "data handler logic element[s]." As discussed above, the specification teaches that the "data handler logic elements" *generate* data patterns. The surrounding claim language does not alter the meaning of "data handler logic elements."[10] Second, the claim's use of "provided" is consistent with Samsung

[10] The "provided" language was added in an amendment during prosecution of the '523 patent on September 5, 2017, which is more than 8 years after the filing of the original application on April 13, 2009. Ex. 6 ['523 FH, Sept. 5, 2017 Amendment] at 2.

and Google's proposed construction, which clarifies that the "data patterns" are *generated* by the data handler logic elements. The data handler logic elements *generate* the "data patterns" before they are "provided" to the "data module" for transmission, as claim 1 requires.

Netlist also argues that Samsung and Google's construction "simply creates another fight about what the word 'generate' means." *Supra* at 39. But this alleged problem has a simple solution (if one is needed). The Court can simply construe "generate" to mean "produce (*i.e.*, bring into existence, including by transformation or modification of information and/or data received from another components)." Netlist agreed to this construction in a prior litigation. *See* Ex. 37 [Inv. No. 337-TA-1023 Initial Determination] at 28–30 (noting that Netlist agreed with the Staff's proposed construction).

Thus, Samsung and Google's proposed construction of "data handler logic element[s]" should be adopted because it adheres to the intrinsic evidence and fits within the broader claim.

3. Netlist's Reply Position

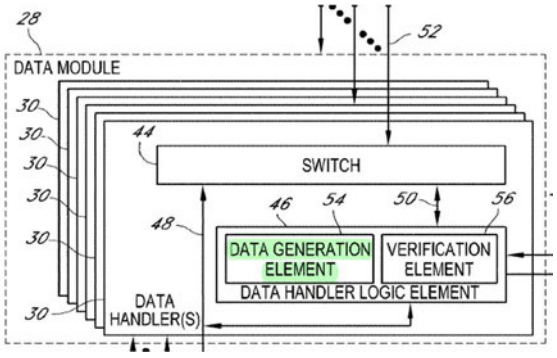
Defendants assert that Netlist's construction does not include a purportedly central feature of the data handler logic elements, *i.e.*, to "generate[] data." *Supra* at 42–. Defendants also argue that "generate" means "produce." *Supra* at 47. That argument, however, ignores the plain language of the claims, which specifies that the data handler logic element "provides," and not "generates" or "produces" data patterns. *See supra* at 38. Defendants claim that they are adding to the claim by importing a generating limitation that is separate from the providing limitation, emphasizing the impropriety of the construction: limitations are not imported from the specification. The specification indisputably describes a data handler logic as a structure that provides data signals. There are also certain non-limiting embodiments in which the logic also generates. The inventors chose to require only certain of these features, as is their right. *See, e.g.*, *Apple Inc. v. Andrea Elecs. Corp.*, 949 F.3d 697, 708 (Fed. Cir. 2020) ("[when] the patent describes multiple embodiments,

every claim does not need to cover every embodiment. This is particularly true [when] the plain language of a limitation of the claim does not appear to cover that embodiment.").

Defendants also ignore the fact that the specification includes embodiments in which data pattern generation is ***not*** a feature of the data handler. For example, the specification states that "***the data patterns of certain embodiments may be programmable*** either through the I^2C interface ***or they may be defaulted to pre-defined values***" '523, 6:23-26 (emphasis added). The specification further states that in "certain embodiments . . . the ***data handlers 30 may be updated through the I^2C interface 15 with new data patterns*** . . . ." '523, 12:38-40 (emphasis added). As another example, the specification discusses a number of functional blocks, including a "data generation element 5," that can be present in a data handler logic element. *See* '523, 38-40. The specification then expressly states that embodiments can omit one or more of these functional blocks:

In various embodiments, the components of the data module **28** (e.g., the switch **44**, the data handlers **30**, the data handler logic element **46**, the data generation element **54**, and/or verification element **56**) may include discrete logic, one or more application-specific integrated circuits (ASICs) one or more microprocessors, one or more field-programmable gate arrays (FPGAs), or one or more computer-programmable logic devices (CPLDs). Additionally, one or more of the various functional blocks (e.g., the switch **44**) of the data module **28** of FIG. **3** may not be included. In some embodiments, additional functional blocks may be included. Moreover, some of the functional blocks are described as separate functional blocks for illustration purposes and may comprise one physical component. For example, in one embodiment, each of the data handlers **30** and the corresponding switch **44**, data generation element **54**, and verification element **56** comprise one physical component (e.g., are included in one integrated circuit package). In another embodiment, the data module **28** comprises one physical component.

'523, 12:43-62



'523, Fig. 3 (excerpt)

In emphasizing that each functional block is optional, the specification expressly contemplates embodiments where the data generation element functional block is excluded from the data handler logic element, data handler, and data module.

The specification also discusses example embodiments that describe the data handler logic element outputting or receiving data signals while making clear that those signals are created by another source. For example, the signals come from the memory devices themselves and are supplied to the data handler logic element (green). And then, those signals may be delivered from the data handler logic element to memory devices. This allows for iterative testing (yellow).

> In certain embodiments, the switch 44 is configured to selectively input to the corresponding plurality of data ports either data signals 48 from the system memory controller 14 or data signals 50 from the data handler logic element 46. The switch 44 of certain embodiments may further be configured to receive ***data signals 52 (e.g., during a read operation) from the plurality of memory devices 18 and to propagate the data signals 52 to the data handler logic element*** 46 and/or the memory ***controller 14. In some embodiments, for example, the switch 44 selectively inputs the data signals 48 to be written to the plurality of memory devices*** 18 from the system memory controller 14 when the memory module 10 is a normal (non-test mode) mode and, alternatively, ***inputs the data signals 50 from the data handler logic element 46 during a test mode.***

'523, 10:17-31.

The vast majority of the extrinsic evidence Defendants cite is not for the '523 patent and often involve patents with different specifications. *Supra* at 44-46. In those references that relate to the '523 patent, the context makes clear that "generate" does not foreclose that the data signal created at a different location from the data logic handler element is provided to the data logic handler element and that the data logic handler element outputs a signal based on the received data signals. *See, e.g.,* Ex. 23 (2022-08-04 Decl. of Michael C. Brogioli) ¶ 25 (rejecting Samsung's construction that "generate" means "produce (i.e., bring into existence)" because "the '523 Patent allows for data handlers to be updated with new data patterns, wherein the data handlers thereafter 'generate' said patterns during a test"). The context of the papers Defendants cite makes clear how "generate" is being used. Defendants, however, refuse to engage what meaning they intend to pour into the term "generate." In specific, Defendants refuse to engage directly as to whether, at a later point in time, their experts will argue that "generate" excludes embodiments such as those at 6:23-

26, 10:17-31, and 10:44-47 in which the data patterns sent by the data handler logic element originate from sources outside the data handler logic element.

4. Samsung and Google's Sur-Reply Position

Netlist continues to conflate one claim limitation, "providing," with another, "data handler logic element[s]." Samsung and Google explained above why Netlist's argument is flawed. Netlist's reply avoids replying to that explanation. Instead of identifying what the claimed "data handler logic element[s]" is, Netlist argues again that it is a generic structure that has no bounds.

Netlist does not dispute that "data handler logic element" has no understood meaning outside of the patent. The patent's specification is particularly informative where the claimed structure is not one known to a person of skill, as here. *See, e.g.*, *Indacon, Inc. v. Facebook, Inc.*, 824 F.3d 1352, 1357 (Fed. Cir. 2016) (because claim terms have no established meaning to a POSITA, they "cannot be construed broader than the disclosure in the specification"); *Howmedica Osteonics Corp. v. Zimmer, Inc.*, 822 F.3d 1312, 1321–22 (Fed. Cir. 2016) ("The meaning of these terms is not facially clear, and a skilled artisan would naturally look to the written description for a full understanding of the claims."). Here, the specification consistently describes the claimed "data handler logic elements" as generating data patterns.

Netlist argues that certain passages of the specification regarding the use of an I^2C bus interface mean that the "data handler logic element[s]" need not generate data patterns. Not so. None of these passages discusses, or even mentions, "data handler logic element[s]." There is also nothing in these passages that is inconsistent with data patterns being generated by a data handler logic element. Specifically, Figure 6 depicts a process in which the test controller is configured via I^2C before data generation is performed at step 214 by the data generation element 54 within the data handler logic elements. '523 patent at 15:42–47. Thus, the specification clarifies that using the I^2C bus does not change the basic requirement that the data handler logic element generates

data patterns. Netlist contends that the patent states, at column 12, lines 43–63, that the data handler logic element need not include a data generation element. But the cited portion of the specification merely states that "one or more of the various functional blocks (e.g., switch 44) of the data *module* 28 of FIG. 3 may not be included." '523 patent at 12:50–52 (emphasis added). The claims here expressly require a "data handler logic element," and as Samsung and Google show above, the data handler logic element generates data patterns in every embodiment.

Netlist also argues that the specification discloses, in column 10, lines 17–31, an embodiment in which "the signals come from the memory devices . . . and then those signals may be delivered from the data handler logic element to memory devices." But, here too, the cited passage does not disclose such an embodiment. Rather, the portion Netlist highlighted in green states that the switch 44 "propagate[s] the data signals 52 to the data handler logic element 46," which is necessary so that a "verification element" can compare the data that is read from the memory devices to the data pattern that was written. '523 patent at 11:16–26. The yellow-highlighted part of the passage describes a separate capability in which the switch 44 either inputs data "from the system memory controller 14 when the memory module 10 is a normal . . . mode" or "from the data handler logic element 46 during a test mode." This passage does not state that the data from a read operation is "delivered from the data handler logic element to memory devices," as Netlist argues. And it certainly does not indicate that the data handler logic element does not generate data patterns—its central aspect as set out by the specification.

Netlist attempts to minimize the numerous statements that it or its experts made previously as extrinsic evidence. *Supra* at 49. But the salient point is that these statements prove that Netlist and its experts have consistently reached the same understanding of the same term. While a number of these statements were made in the context of the '434 patent, arguing that this patent has a

"different specification" is baseless. The '523 patent is a child of the '434 patent via a series of continuation applications. *See* '523 patent at 1:7–26. Thus, the written description in the '523 patent's specification must be the same. In addition, Netlist and its expert, Dr. Brogioli, repeated these statements regarding the '523 patent in this action, Ex. 11 [Brogioli Decl.] ¶ 30, and before the Patent Office, Ex. 23 [Brogioli Decl. ISO POR] ¶ 53–54.

Netlist's argument that Samsung and Google "refuse to engage directly" regarding the meaning of "generate" is difficult to reconcile with the record. Samsung and Google have agreed to use a meaning for "generate" that Netlist has agreed to use in a prior litigation. Thus, any alleged confusion over "generate" can be easily resolved by adopting Netlist's prior definition. Further, Netlist's argument that Samsung and Google will use "generate" to exclude embodiments with I^2C misunderstands the specification. As explained above, the "data handler logic element[s]" must still generate the data patterns for embodiments in which an I^2C bus is used to configure the test. *See, e.g.*, '523 patent at 15:42–47.

E. "data handler[s]" (cls. 2, 4, 5, 8, 9, 10–11, 19, 20, 23–24, 26, 28–32, 34)

Samsung & Google's Proposed Construction	Netlist's Proposed Construction
"circuitry for generating and processing data"	"a component containing the data handler logic element[s]"

1. Netlist's Opening Position

The term "data handler" only appears in either dependent claims or in claim 19 as part of the recitation of the data handler logic element circuitry. The claims expressly describe the functions performed by the data handler. For example, claim 2 provides:

> 2. . . . wherein the data module includes a plurality of data handlers, each respective data handler of the plurality of data handlers including a respective one of the data handler logic elements, wherein the each respective data handler is configured to propagate a respective n-bit section of the each data signal of the one or more first data signals between the system memory controller and a respective memory device

> group of the plurality of memory device groups, n being a fraction of N, and wherein the each respective data handler is further configured to output a respective n-bit wide section of each of the one or more second data signals including one or more respective n-bit-wide data patterns provided by the respective one of the data handler logic elements to the respective memory device group. Ex. 1 ('523 Patent) at cl. 2; *see also, e.g.*, cls. 4, 5, 11, 19, 20, 23, 24, 26, 29-32.

Adding the ambiguous functions of "generating and processing data" to the already recited functions in the claims does nothing but add ambiguity. Assigning a generating function to the data handler is particularly inappropriate because, as discussed above, only one of multiple embodiments recites this function as present in the data handler. The specification teaches that data handlers include data hander logic elements. *Id.* at 10:6-36. Because the structure of data handler logic elements is already defined above, there is no need for additional construction beyond the specifications teaching that the data handler is a component of the data module:

> In various embodiments, the components of the data module 28 (e.g., the switch 44, the data handlers 30, the data handler logic element 46, the data generation element 54, and/or verification element 56 . . . . *Id.* at 12:43-45.

2. Samsung and Google's Answering Position

Samsung and Google's proposed construction fully captures the "data handler" by including both a requirement that it includes "circuitry for generating . . . data," i.e., includes the "data handler logic elements," *and* includes "circuitry for . . . processing data." As explained above for "data handler logic elements," the intrinsic record requires the "data handler" to include "circuitry for generating . . . data," and Netlist has repeatedly emphasized this function.

In addition, the intrinsic record requires the data handler to include circuitry for "processing data," which is necessary for the operation of the "data handler." For example, Figure 3 of the '523 patent depicts a data module that includes "data handlers 30." *Id*. at 9:32–34, 10:7–10. In Figure 3, each of the data handlers 30 includes a switch 44, which is separate from the "data handler logic elements." *Id.* at 10:13–36. The switch may process data in several ways:

- "may provide a bi-directional data multiplexor function."
- "selectively input to the corresponding plurality of data ports either data signals 48 from the system memory controller 14 or data signals 50 from the data handler logic element 46."
- "receive data signals 52 (e.g., during a read operation) from the plurality of memory devices 18."
- "propagate the data signals 52 to the data handler logic element 46 and/or memory controller 14."
- "selectively inputs the data signals 48 to be written to the plurality of memory devices 14 when the memory module 10 is a normal (non-test mode) mode."
- "inputs the data signals 50 from the data handler logic element 46 during test mode."

Id. Each of these functions describe operations that occur outside of the "data handler logic element[s]," evidencing that Netlist's construction improperly reads out structures and functions of the "data handler(s)." To complete the construction of "data handler," Samsung and Google have captured these operations within their proposed construction as "processing data."

Netlist similarly described the dual function of the "data handler" at the hearing in 337-TA-1023. According to Netlist, the "apparatus taught" in the specification comprises data handlers that "control the movement of the data from the memory controller - to and from the memory controller and the memory devices" and "provide generation of signals to help with the self-tests." Ex. 36 [Inv. No. 337-TA-1023 Hearing Tr.] at 36–37.

Samsung and Google's proposed construction is also consistent with Judge Albright's construction of "data handler" in prior litigation in the Western District of Texas between Netlist and SK hynix. Netlist concedes that Judge Albright construed "data handler" as "circuitry for generating and processing data"—identical to Samsung and Google's proposed construction. *See* Ex. 17.

Netlist's proposed construction describes only part of the "data handler"—*i.e.*, the part that includes the "data handler logic elements." But, as explained above, Figure 3 shows that the "data handler" includes the "data handler logic elements" and functionality outside the "data handler logic elements" for processing data. Thus, Netlist's proposed construction is incomplete, and Samsung and Google's proposed construction should be adopted.

3. Netlist's Reply Position

As noted above, data *generation* is not a required feature of the "data handler": while some of the embodiments ascribe data generation to the "data handlers," others ascribe this feature to the "data module" as a whole, some ascribe the data as originating via the host via I^2C interface, and still others say nothing about data generation per se. *See supra* at 38-39, 48-49. Thus, it is improper to rewrite the claims to require that the "data handler" generate data.

Defendants' construction also seeks to rewrite "data handler" to require "processing data." This construction is flawed for two reasons. First, the only intrinsic evidence they cite to support this aspect of the construction are citations to a particular sub-embodiment of the invention found in col 10 lines 13-36 that describes how the data handler depicted in Fig. 3 may include a switch for routing data. As highlighted above, the specification expressly states that any of the functional blocks depicted in the data module of Fig. 3 may not be present. *See* '523, 12:43-62.

The second issue is the proposed constructions begs the question of what "processing" data means. *See supra* at 53-54. Defendants base that aspect of the construction on the functions described for the switch in 10:13-36. But none of the cited passages mention "processing" or "process" data. Rather, those functions relate to the movement of the data, as Netlist characterized in the 1023 ITC action. *See supra* at 53-54 (citing Ex. 36); *see also* '523, 10:13-36. Defendants' characterization of those stated functions as "processing" data can mislead the jury into believing "processing" data requires transforming or modifying the data.

Defendants' citation to a technology tutorial of a prior ITC proceeding (Ex. 36) does not support their construction as Netlist there highlighted embodiments that were pertinent to the claims at issue in that case and did not purport to provide a definitive construction of the term "data handler." Additionally, the statements before the ITC do not support Defendants' use of the term "processing," as there Netlist stated that the data handlers in the relevant embodiments "control the movement of the data." Again, the term "processing" injects unnecessary confusion and derivative claim construction issues.

4. Samsung and Google's Sur-Reply Position

The parties agree that "data handlers" functionally "contain the data handler logic element." Samsung and Google's construction, consistent with their construction for "data handler logic element[s]," requires the data handler to include "circuitry for generating" data.

Netlist argues that Samsung and Google seek to rewrite data handler to require processing data, but this is a core required capability of the data handler. Netlist's proposed construction would omit this function from the data handler, but claim 19 illustrates the problem with Netlist's proposal. The "data handler" in claim 19 must be able to "propagate one or more data signals" and "provide respective data patterns" that are generated by the "data handler logic element" within it. While including the "data handler logic element," as Netlist proposes, would allow the "data handler" to perform the second function, it is not sufficient to perform the first. There is no embodiment in which the "data handler logic element" is used to perform the recited function in the claimed "first mode." Thus, "processing" data must be included in the "data handler" in order to support the claimed "first mode."

Netlist separately argues that including "processing" in the "data handler" construction "can mislead the jury" and "inject[] unnecessary confusion and derivative claim construction issues." Netlist's concerns are unfounded. Samsung and Google have already explained that the

operation of switch 44 during normal mode is an example of "processing" data. There is no reason to believe that the jury would spontaneously require "transforming or modifying the data."

F. "first memory address and control signals" / "second memory address and control signals" / "third memory address and control signals" (cls. 1, 4, 13, 16)

Samsung & Google's Proposed Construction	Netlist's Proposed Construction
"first, second and third memory address and control signals must be memory address and control signals having different frequencies"	plain and ordinary meaning, that is, respectively, first, second and third memory address and control signals

1. Netlist's Opening Position

Samsung/Google attempt to inject additional requirements into the above claims that have no basis in the claims, specification, or prosecution history.

The claims outline three memory address and control signals, with no implication that they must have different frequencies. The "first memory address and control signals" are output by the control module to the memory devices in the first mode. These signals are used to coordinate the reading of data from—and the writing of data to—the memory devices during typical DIMM operation:

> wherein the control module in the first mode is configured to receive system address and control signals from the system memory controller and to output first memory address and control signals to the memory devices according to the system address and control signals, and the data module in the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller, the one or more first data signals being transmitted or received by at least a portion of the memory devices in response to the first memory address and control signals . . . . Ex. 1 ('523 Patent) at cl. 1.

The "second memory address and control signals" are output by the control module to the memory devices in the second mode. These signals coordinate the writing of "second data signals" into specific memory devices:

> wherein the control module in the second mode is configured to output second memory address and control signals to the address and control ports of the memory devices, and the data module in the second mode is configured to isolate the memory devices from being accessed by the system memory controller and to transmit one or more second data signals including data patterns provided by the data handler logic elements to the data ports of the memory devices according to one or more commands output from the control module, and wherein at least a portion of the memory devices are configured to receive the one or more second data signals according to the second memory address and control signals from the control module. *Id.*; *see also* cls. 13, 16.

Finally, under dependent claim 4, the control module also outputs "third memory address and control signals" to the memory devices in the second mode. These signals coordinate the reading of the data that was written into the memory devices back to the data handlers so they can be checked.

> 4. The memory module of claim 2, wherein the control module is configured to output third memory address and control signals to the address and control ports of the memory devices during the second mode, the third memory address and control signals causing the memory devices in one of the at least one rank to output at least one N-bit wide read data signal, and wherein the each respective data handler is configured to receive a respective n-bit section of each of the at least one N-bit wide read data signal. *Id.* at cl. 4; *see also* cl. 5.

None of these functions require a change of signal frequency. The first and second signals are delivered in different modes, and this is what distinguishes them. The second and third signals are delivered in the same mode, but the third signals have an additional requirement, "causing the memory devices in one of the at least one rank to output at least one N-bit wide read data signal." This is what distinguishes the second from third signals.

The specification explicitly describes embodiments in which signals used during one mode have the same operating speed, or frequency, as those used during a different mode of operation of the DIMM.

> **The data module 28 and/or the control module 22 of certain embodiments are configured to test the plurality of memory devices 18 at *the* normal operating speed of the memory devices 20**. For example, the data module 28 and/or the control module 22 are configured to provide memory signals (e.g., data, address

> and control signals) according the operating specification of the memory devices 20. In some embodiments, the control module 22 and the data module 28 produce memory addresses, control and/or data signals according to the JEDEC standard memory protocol. *Id.* at 6:7-18.

The definite article "the" contemplates that there is a single operating speed. This is consistent with DIMMs at the time. *See, e.g.*, Ex. 43 (JEDEC DDR2 SPD Specification) at 1 (byte 9 of each DDR2 DIMM's SPD reporting DIMM's "SDRAM cycle time"). The specification describes as non-limiting examples a "test" mode and a "normal" mode, which can be examples of a first and second mode. *See id.* at 2:38-40. As established in the above quotation, in certain embodiments, the same "normal operating speed" is employed in both of these modes.

The specification also describes an alternative embodiment where the signals used during testing are higher or lower frequency than typical:

> ***In some embodiments***, the data module **28** and/or the control module **22** are configured to test the plurality of memory devices **18** under non-normal conditions. ***For example***, the data module **28** and/or control module **22** may be configured to provide signals having frequencies which are higher or lower than the normal operating frequencies of the memory devices **20**. *Id.* at 6:36-42.

Samsung/Google's construction attempts to clumsily import this specific example embodiment into the claims. But under this embodiment, all signals used during the "test" mode would have the same frequency; in contrast, Samsung/Google's construction requires the second and third memory address and control signals have different frequencies.

2. Samsung and Google's Answering Position

By reciting a "first," "second," and "third" memory address and control signals, the claims use a "common convention" to confirm that the "first," "second," and "third" memory address and control signals must each be different "memory address and control signals." The use of the terms "first," "second," and "third" as qualifiers for the "address and control signals" terms "is a common patent-law convention to distinguish between repeated instances of an element or limitation."

3M Innovative Props. Co. v. Avery Dennison Corp., 350 F.3d 1365, 1371 (Fed. Cir. 2003). In *3M*, the terms "first" and "second" were used to connote *distinct* "patterns" in a method for embossing a film. *Id*. The same result was found in *Gillette Co. v. Energizer Holdings, Inc.*, where the terms "first, second, and third" were held to "distinguish different elements of the claim." 405 F.3d 1367, 1373 (Fed. Cir. 2005); *see also*, *e.g.*, *Free Motion Fitness, Inc. v. Cybex Int'l, Inc.*, 423 F.3d 1343, 1348 (Fed. Cir. 2005) ("first pivot point" is distinct from "second pivot point"); *Newtech Touch-Up Sys., Inc. v. Front Line Ready GA LLC*, No. 09-cv-5158-RBL, 2010 WL 5394962, at *3–5 (W.D. Wash. Dec. 23, 2010) (construing claim reciting a "first cloth," "second cloth," "third cloth," and "fourth cloth" to require "four separate cloths"). This common convention applies here. The three memory address and control signals, in plain language, refer to distinct signals.

The structure of the claims confirms this reading, as each of the three distinct memory address and control signals are generated using different information and defined in the claims to serve a different purpose. For example, claim 1 uses the terms "first" and "second" to define distinct address and control signals. As Netlist admits, the "'first memory address and control' signals are output by the control module to the memory devices in the *first mode*" and "are used to coordinate the reading of data from—and the writing of data to—the memory devices during typical DIMM operation." *Supra* at 57 (emphasis added). In contrast, as Netlist also admits, the "'second memory address and control signals' are output by the control module to the memory devices in the *second mode*" and "coordinate the writing of 'second data signals' into specific memory devices." *Supra* at 57 (emphasis added). Claim 1 makes clear (and Netlist agrees) that the "first mode" and the "second mode" are two different modes—"the first mode is configured to propagate one or more first data signals between the memory devices and the system memory controller" while the "second mode is configured to isolate the memory devices from being

accessed by the system memory controller and to transmit one or more second data signals." D.I. 145 [Joint Claim Construction Chart] at 4 (Netlist's proposed construction for "first mode" is "a mode that differs from the 'second' mode").

Similarly, the third memory address and control signals also differ from the first and second signals. Claim 4—the only claim that requires a "third" memory address and control signals—similarly dictates that this "third" memory address and control signals are distinct from the "first" and "second" memory address and control signals of claim 1. Unlike the "first" and "second" memory address and control signals in claim 1, Netlist admits that the "third" memory address and control signals of claim 4 "coordinate the reading of the data that was written into the memory devices back to the data handlers so they can be checked." *Supra* at 58.

Nothing in the claim language suggests the "first," "second," and "third" address and control signals may comprise the same address and control signals. Indeed, Netlist agrees that the first and second memory address and control signals are different, because the first and second memory address and control signals "are delivered in different modes, and [that] is what distinguishes them." *Supra* at 58. Netlist also agrees that even though the "second and third signals are delivered in the same mode, [] the third signals have an additional requirement," which "is what distinguishes the second from third signals." *Id*.

Despite this apparent agreement, Netlist contends that the plain and ordinary meaning is just "first, second and third memory address and control signals." To the extent this means the first, second, and third signals can be the same signals, it would render the "first," "second," and "third" language meaningless. A construction that renders words superfluous and meaningless is rarely correct. *See Harris Corp. v. IXYS Corp*., 114 F.3d 1149, 1152 (Fed. Cir. 1997) (rejecting

construction that "would contribute nothing but meaningless verbiage to the definition of the claimed invention"). Netlist's construction should thus be rejected.

The '523 patent does not include a detailed description of how the claimed address and control signals might differ. For example, the patent does not include a figure depicting the different signals. The only concrete description of how signals might differ is found in column 6 lines 36 to 42. In this passage, the specification explains that the "data module 28 and/or control module 22 may be configured to provide signals having frequencies which are higher or lower than the normal operating frequencies of the memory devices 20." In other words, this passage describes having signals that have different frequencies: "normal operating frequencies" and "frequencies which are higher or lower" than that. Samsung and Google's construction is consistent with the only relevant description in the '523 patent. *See Medicines Co.*, 853 F.3d at 1309 (construing "efficient mixing" based on "the only *description* of efficient mixing in the patents in suit").

Netlist argues that the '523 patent discloses an embodiment in which a single operating speed is used. *Supra* at 58–59. Even assuming that Netlist is correct, the patentee chose to use "first," "second," and "third" indicators before "memory address and control signals." The presence of these indicators requires the signals to be different and demonstrates that the patentee chose to limit the claims to embodiments in which the signals are different.

3. Netlist's Reply Position

Netlist agrees that "first," "second," and "third" "memory address and control signals" are each separate signals that are physically distinct from one another. Netlist cannot point to one signal and say it is all three signals. That the first, second, and third signals are physically distinct does not mean the frequency of each is necessarily different. Three signals, each with the same frequency, can be sent. What makes the signals different is that each of the signals performs a

different function depending on the mode of the control module, as recited in the claims. *See supra* at 57-58.

Defendants' case law does not support importing a different frequency limitation into the claim. In *3M*, the dispute was about whether "first" and "second" patterns demanded a particular temporal sequence. *3M Innovative Properties Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1371 (Fed. Cir. 2003). The court held that both the "first" and "second" patterns could be identical in nature in that the specification defined both of them as "superimposed." It simply required that there be two such superimposed patterns, not that they be different in some other way, such as temporally:

> In the specification, 3M clearly acted as its own lexicographer, and the definition provided requires only that the "two or more embossing patterns" be "superimposed." '930 patent, col. 2, ll. 1-2. Despite Avery's arguments to the contrary, the use of "superimposed" in this definition neither transforms claim 1 into a product-by-process claim nor even limits the scope of the claim to a serial method of manufacture . . . .

Id. at 1371. The Federal Circuit makes clear that the ordinal terms "first," "second," and "third" can be used when describing different instances of an identical structure. For example, if first, second, and third apples are claimed, there need be three apples, but they can all be Fuji apples:

> The use of the terms "first" and "second" is a common patent-law convention to distinguish between repeated instances of an element or limitation.

Id. In fact, ordinal claiming is employed because the "first," "second," and "third" elements may be identical except for the fact that there are three of them. So, too, here, the court need not impose an additional limitation to distinguish the signals when the plain language of the claims makes clear how the three signals are distinct.

In *Gillette*, the court rejected an argument that "first," "second," and "third" blades limit the claim to have three specific blades. *Gillette Co. v. Energizer Holdings, Inc.*, 405 F.3d 1367, 1373 (Fed. Cir. 2005). The court explained that the different functions of each of the three recited

blades were "defined by the clear language of the claim," and it was improper to import any other limitation into the use of "ordinal" terms. *Id.*

Free Motion Fitness is of a piece, emphasizing that ordinal claim language allows for multiple appearances of an identical structure: "As we have previously held, '[t]he use of the terms `first' and `second' is a common patent-law convention to distinguish between repeated instances of an element or limitation.'" *Free Motion Fitness, Inc. v. Cybex Int'l, Inc.*, 423 F.3d 1343, 1348 (Fed. Cir. 2005). In that case, claims defined the different functions of the "first pivot point" and "second pivot point," and it was held improper to import any other limitations into the terms. *Id.*

4. Samsung and Google's Sur-Reply Position

Netlist concedes that by reciting "first," "second," and "third" memory address and control signals, the claims use a "common convention" to confirm that the "first," "second," and "third" memory address and control signals must each be different "memory address and control signals." While Netlist theorizes there could be other ways in which these signals differ, the specification's only concrete description of how these signals might be "different" is found in column 6, lines 36–42, which describes signals having different frequencies. Since Samsung and Google's construction is consistent with the only relevant description in the '523 patent, it should be adopted.

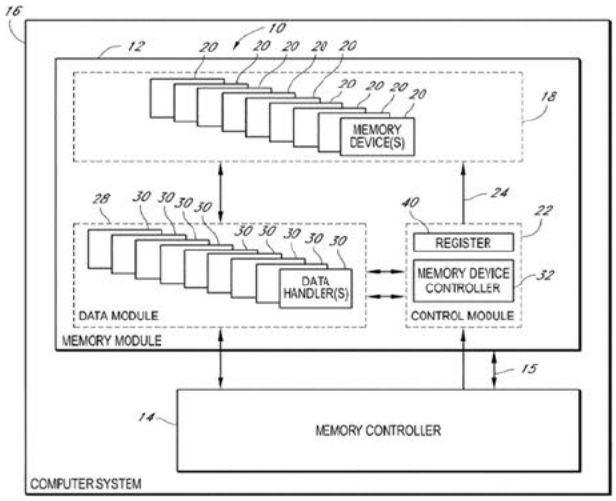
Netlist's attempt to "distinguish" Samsung and Google's cited cases does not show otherwise. The Federal Circuit rejected attempts by parties, like Netlist, to use "first," "second," and "third" to indicate something ***other*** than that the elements were different. *3M*, 350 F.3d at 1371 ("first" and "second" connote distinct things, but not an ordering sequence); *Gillette*, 405 F.3d at 1373 ("first," "second," "third" blades connote distinct things, but not a consecutive, numerical limit of blades); *Free Motion*, 423 F.3d at 1348 ("first pivot point" and "second pivot point" connote distinct things, but not the relative position of multiple pivot points).

G. "disposed on the circuit board at a position corresponding to" (cls. 9, 28)

Samsung & Google's Proposed Construction	Netlist's Proposed Construction
"disposed on the circuit board at a position corresponding to" means "physically closer to the group of memory devices than any other memory devices" Otherwise, this term is indefinite.	plain and ordinary meaning, that is, "wherein the multiple data handlers include physically separate integrated circuit packages, and wherein the each respective data handler is placed on the circuit board at a position corresponding to the respective memory device group" / "wherein the multiple data handlers include physically separate integrated circuit packages, and wherein the each respective data handler is placed on the circuit board at a position corresponding to the respective group of one or more memory devices"

1. Netlist's Opening Position

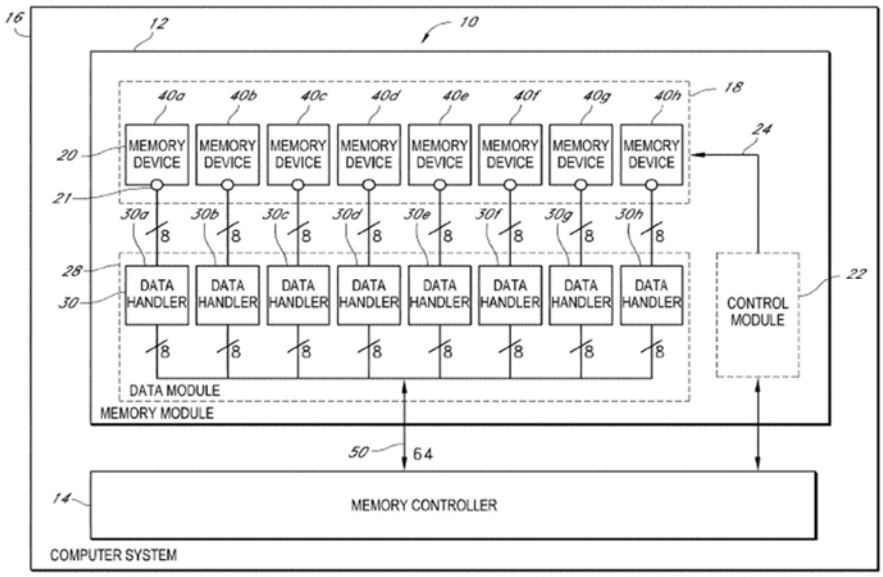
The plain language of dependent claims 9 and 28 requires positional correspondence between each data handler and its associated memory device group on the PCB. Figure 1 shows memory devices and data handlers arrayed diagonally on the memory module, where each respective data handler (30) has a corresponding memory device (20). But neither the figure nor the specification require that the corresponding handler have any particular physical location relative to any other handler or memory device.



The specification further describes this correspondence in general terms:

> Each data handler **30** is operable independently from each of the other data handlers **30** of the plurality of data handlers **28** and is operatively coupled to a corresponding plurality of the data ports of one or more of the plurality of memory devices **18**. *Id.* at '523 at 5:16-20.

Figure 2 of the patent shows a second possible embodiment. Samsung/Google will argue that 30h is closest 40h, 30g is closest to 40g, etc. First, under Federal Circuit precedent, a figure is not to be used to depict physical measurements unless the specification makes clear that it is so intended. *See Nystrom v. TREX Co.*, 424 F.3d 1136, 1149 (Fed. Cir. 2005) ("The district court erred in not properly applying the principles set forth in our prior precedents that arguments based on drawings not explicitly made to scale in issued patents are unavailing."); *see also Application of Wright*, 569 F.2d 1124, 1127 (C.C.P.A. 1977) ("Absent any written description in the specification of quantitative values, arguments based on measurement of a drawing are of little value.").



In this case, the specification expressly warns: "The configuration shown in FIG. 2 is ***for the purposes of illustration and is not intended to be limiting***." *Id.* at 8:62-63. The specification makes clear there can be positional correspondence based on features other than what handler is "closer" to the memory device.

> ***In certain embodiments***, each of the plurality of data handlers **30** is positioned on the PCB **12** proximate to the corresponding plurality of data ports. For example, each data handler **30** ***of certain embodiments*** is positioned closer to the corresponding plurality of data ports **21** than the data handler **30** is to the other data ports **21** of the plurality of memory devices **18**. For example, the data handler **30** *a* is positioned closer to the corresponding plurality of data ports **21** of the memory device **40** *a* than to the other data ports **21** of the other memory devices **40** *b*-**40** *h*. *Id.* at 9:22-31.

The claims do not use the "closer" limitation.

The prosecution history further supports Netlist's position that proximity is only one possible way a data handler can correspond to its respective memory device group. In a February 15, 2018 Amendment, Netlist amended the claims to eliminate language similar to the construction Samsung/Google are now proposing:

> 12. (Currently Amended) The memory module of claim 2, wherein the plurality of data handlers include physically separate integrated circuit packages, and wherein the each respective data handler is ~~positioned~~ disposed on the circuit board at a position corresponding ~~proximate~~ to the respective memory device group.

Ex. 9 (2018-02-15 Amendment) at 5, 9 (amendment to claim 62, renumbered to 28 in the final claims). To support this and other amendments, Netlist cited the specification and drawings. See *Id.* at 13. The examiner rejected other claims as indefinite but found that this amendment was allowable. Ex. 10 (2018-04-10 Office Action) at 6. Samsung/Google are seeking a construction that undoes this claim amendment.

In the PTAB, Samsung did not advance its physical proximity construction via a proposed claim construction, or even in its analysis of the limitation. *See* Ex. 19 (Petition, IPR2022-00063) at 13-15, 81-81. In the analysis of the limitation, the fact that the switch is *below* the memory device it is connected to showed the limitation is met.

b) [9/28.b] Corresponding Positions

FIGS. 5-6 show each Switch ASIC positioned below its corresponding memory devices disposed on either side of the PCB ("*disposed on the circuit board at a position corresponding to the respective memory device group*").

EX1003,¶434; EX1005,¶¶[0003],[0047].

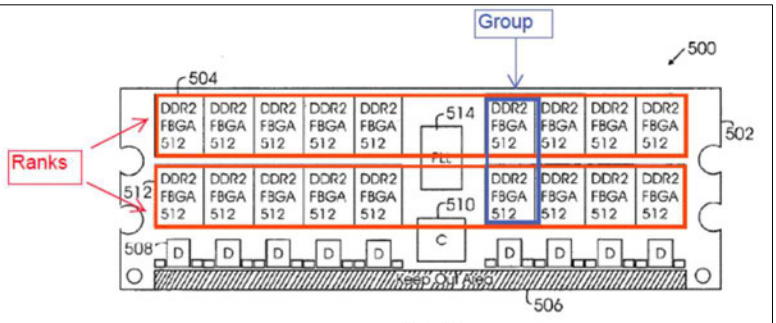


Fig. 5

The text accompanying FIGS. 5-6 confirms each Switch ASIC corresponds to the memory devices above it, and corresponding FIG. 2 shows each Switch ASIC is positioned nearest to its "*memory device group.*" EX1003,¶435; EX1005,¶¶[0048-0050].

Samsung/Google assert that if their construction is not adopted, the terms are indefinite. Samsung/Google never fully explained this position in meet and confer. But the fact that a term can potentially apply broadly, or even require dueling expert testimony, does not make a term indefinite. *See BASF Corp. v. Johnson Matthey Inc.*, 875 F.3d 1360, 1367 (Fed. Cir. 2017) ("[T]the inference of indefiniteness simply from the scope finding is legally incorrect: 'breadth is not indefiniteness.'"); *Eli Lilly & Co. v. Teva Parenteral Medicines, Inc.*, 845 F.3d 1357, 1370-72 (Fed. Cir. 2017) (affirming district court's determination of definiteness in light of patentee's expert's testimony, notwithstanding contrary expert testimony from accused infringer's expert). In this case, the "position corresponding" language is modified by the concept of "group." And each figure shows that each group is connected to a data handler that is not shared with at least one other group. Netlist has submitted a declaration of Dr. Michael C. Brogioli analyzing the definiteness of the limitation. *See* Ex. 11.

2. Samsung and Google's Answering Position

Dependent claims 9 and 28 state that the plurality of data handlers "include physically separate integrated circuit packages," wherein "each respective data handler is ***disposed on the circuit board at a position corresponding to*** the respective [memory device group / group of one or more memory devices]." Samsung and Google propose that the italicized language above means "physically closer to the group of memory devices than any other memory devices." Netlist avoids defining the disputed phrase; instead, it argues that the data handler of claims 9 and 28 does not need to have "***any particular physical location*** relative to any other handler or memory device." *Supra* at 65 (emphasis added). Samsung and Google's proposed construction is consistent with the claim language and specification. Netlist's interpretation should be rejected because it ascribes no meaning to the disputed limitation and renders claims 9 and 28 indefinite.

a) The Specification Confirms That "Disposed on the Circuit Board at a Position Corresponding to" Refers to Physical Proximity

Figure 2, reproduced below (annotated), provides a diagram of an exemplary self-testing memory module. It depicts memory module 10, which includes a control module 22 that generates address and control signals for testing memory devices 20 and data module 28 with a plurality of data handlers 30. *See, e.g.*, '523 patent at 5:12–16. In this example, each data handler 30 (*e.g.*, data handlers 30*a*-30*h*) has an associated memory device 20 (*e.g.*, memory devices 40*a*-40*h*). The data handlers 30 generate test patterns to write to memory devices 20, and compare test patterns read from memory devices 20 to the written patterns to identify faults. *See, e.g.*, *id*. at 5:28–34.

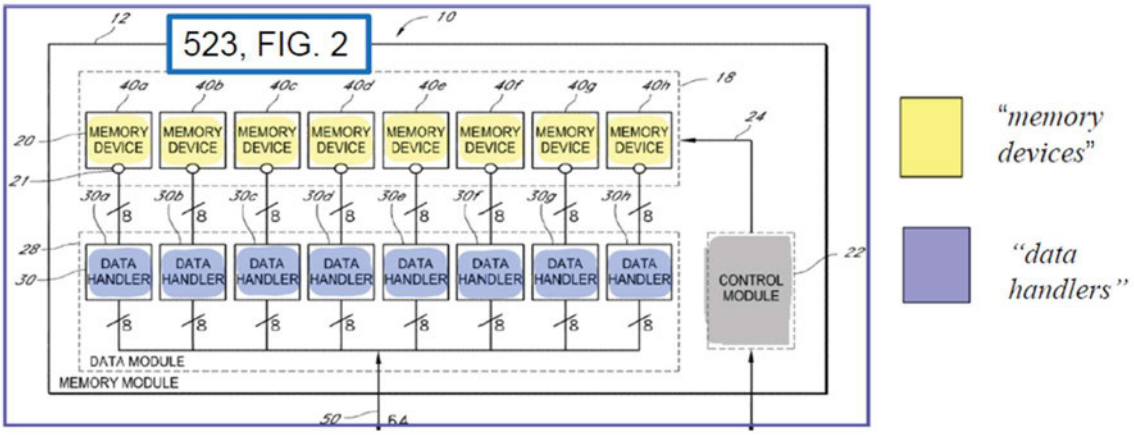


Figure 2 does not depict a physical layout of these various components on a circuit board,[11] but the specification provides guidance that supports Samsung and Google's proposed construction. Specifically, column 9 of the specification states:

> In certain embodiments, each of the plurality of data handlers 30 is positioned on the PCB 12 proximate to the corresponding plurality of data ports. For example, each data handler 30 of certain embodiments is positioned closer to the corresponding plurality of data ports 21 than the data handler 30 is to the other data ports 21 of the plurality of memory devices 18. For example, the data handler 30*a* is positioned closer to the corresponding plurality of data ports 21 of the memory device 40*a* than to the other data ports 21 of the other memory devices 40*b*-40*h*.

'523 patent at 9:22–31. This passage is the only portion of the specification that describes the placement of a data handler relative to its corresponding memory device group. Notably, it suggests that "disposed on the circuit board at a position corresponding to" refers to *physical* proximity. Netlist contends that this portion of the specification does not govern because it uses non-limiting language (*e.g.*, "certain embodiments"). *Supra* at 66–67. But non-limiting language

[11] Netlist and its expert, Dr. Brogioli, appear to believe that the figures in the patent depict the *physical* placement of components on the circuit board. For example, in discussing Figure 1, Dr. Brogioli states that it "shows memory devices and data handlers arrayed diagonally on the memory module." *Supra* at 65; Ex. 11 [Brogioli Decl.] ¶ 35. In discussing Figure 2, Netlist suggests that it shows memory devices and data handlers positioned across from one another in rows. *Supra* at 66; Ex. 11 [Brogioli Decl.] ¶ 35. These figures, however, are block diagrams and would not be understood to show a physical circuit board layout. In the case of Figure 1, it would make no sense to stack packages on top of one another in a diagonal array.

alone cannot justify expanding the scope of the claims beyond what the inventors described as their invention. *See Bell Atlantic*, 262 F.3d at 1269–75; *Medicines Co.*, 853 F.3d at 1307–09. Tellingly, Netlist cannot identify *any other* embodiment or statement in the specification that sheds light on the meaning of the disputed limitation, which claims a "position."

The claim language confirms that the physical location is a limitation. Claim 9 requires that the "data handler is *disposed on* the circuit board *at a position* corresponding to" memory devices. Both "disposed on" and "position" indicate that this limitation addresses the physical location of a data handler relative to a memory device group.

Netlist's own interpretation of similar claim language in a prior ITC action involving a different Netlist patent also supports Samsung and Google's proposed construction. There, Netlist argued that the phrase "each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more [first and second] memory devices" requires "***physical close-ness***." Ex. 38 [Inv. No. 337-TA-1089, Initial Determination] at 98–100. The ALJ agreed, noting that the specification of the patent-at-issue taught that "in a position corresponding to" refers to physical "alignment" of each buffer circuit and its respective one or more memory devices. *Id*. In the case of the '523 patent, the specification also provides a teaching that informs the meaning of the claims: "disposed on the circuit board in a position corresponding to" means "physically closer to the group of memory devices than any other memory devices."

Netlist argues against Samsung and Google's proposed construction by pointing to the prosecution history, where the applicant modified the language of these claims. *Supra* at 67. But the prosecution history merely reflects Netlist's litigation driven attempts to amend the claims. Netlist amended the claims *sua sponte* at the eleventh hour in an attempt to avoid issues that arose during Netlist's litigation with SK hynix. Specifically, in litigation involving Netlist's U.S. Patent

No. 8,001,434—the parent to the '523 patent—SK hynix argued that the phrase "wherein each of the plurality of data handlers is positioned on the printed circuit board proximate to the corresponding plurality of data ports" is indefinite.[12] Ex. 39 [Mangione-Smith Rebuttal Rpt.] at NL-SS-1453_00062785]. Presumably hoping to avoid facing such a challenge in the future, Netlist *sua sponte* amended the pending '523 patent claims as follows: "wherein the each respective data handler is ~~positioned~~ disposed on the circuit board at a position corresponding ~~proximate~~ to the respective memory device group." Ex. 8 ['523 FH, Feb. 8, 2018 Amendment] at 5, 9. Netlist stated that support for the amendment is "found throughout the Specification and Drawings" and certified that the amendment did not add "new matter" to the claims. *Id*. at 12. If Netlist's representations were accurate, "disposed at a position corresponding to" must refer to physical proximity, because that is the only interpretation that finds support in the specification, as set out above. Otherwise, as explained below, the claims are indefinite because there is no other support for this phrase.

Finally, Netlist is wrong to suggest that Samsung did not apply its "physical proximity" construction in its analysis of claims 9 and 28 during the '523 patent IPR proceeding. *Supra* at 67–68. Netlist's excerpt from Samsung's petition contradicts Netlist's assertion, as it plainly states: "FIG. 2 shows each Switch ASIC is positioned ***nearest to*** its "memory device group." *Id*. Further, Netlist ignores the more detailed opinions and support discussed in the accompanying expert declaration. Ex. 24 [IPR2022-0063, Subramanian Decl.] ¶¶ 433–38 ("FIG. 2 of Ellsberry confirms that each Switch ASIC is positioned nearest the memory device group coupled to the Switch ASIC."). Thus, Samsung's interpretation of this phrase in IPR proceedings is consistent with the construction proposed here.

[12] In arguing against indefiniteness, Netlist's expert pointed *only* to the description in column 9 of the specification, discussed above. Ex. 39 [Mangione-Smith Rebuttal Rpt.] at NL-SS-1454_00062785.

b) If Samsung and Google's Proposed Construction Is Not Adopted, Claims 9 and 28 Are Indefinite

"A patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). "[P]atent claims with descriptive words . . . must provide objective boundaries for those of skill in the art in the context of the invention to be definite." *Niazi Licensing Corp. v. St. Jude Med. S.C., Inc.*, 30 F.4th 1339, 1349 (Fed. Cir. 2022) (cleaned up). "[T]he intrinsic record—the patent's claims, written description, and prosecution history—along with any relevant extrinsic evidence can provide or help identify the necessary objective boundaries for claim scope." *Id*.

If, as Netlist argues, claims 9 and 28 do not require a data handler to have "any particular physical location relative to any other handler or memory device," *supra* at 65, these claims are indefinite. A skilled artisan would lack the guidance required to determine whether each respective data handler is "disposed on" the circuit board "***at a position corresponding to***" the respective memory device group, and would be left to wonder: what type and/or degree of "correspond[ence]" is sufficient to satisfy the claims? *See, e.g.*, *Geoscope Tech. Pte. Ltd. v. Google LLC*, No. 22-cv-01331-MSN-JFA, 2023 WL 4627433, at *11 (E.D. Va. Jul. 19, 2023) (holding term "in proximity" is indefinite, where patent holder could not identify any particularized guidance from intrinsic evidence that would enable a POSITA to understand, with reasonable certainty, what "in proximity" means in context of invention).

Netlist's attempt to resolve the ambiguity of claims 9 and 28, without reference to column 9 of the specification, collapses under scrutiny. The declaration from Netlist's expert, Dr. Brogioli, demonstrates that, in his opinion, claims 9 and 28 encompass virtually *any* placement of data

handlers and memory device groups on the circuit board. *See* Ex. 11 [Brogioli Decl.] ¶¶ 36–37. Indeed, Dr. Brogioli does not identify a circuit board layout that would *not* satisfy the claims. Netlist and its expert simply maintain that there is a reasonably discernible boundary to these claims because "each group of memory devices is connected to a data handler that is not shared with at least one other group of memory devices." *Supra* at 68; Ex. 11 [Brogioli Decl.] ¶ 38. But this interpretation of "correspond[ence]" is made out of whole cloth and gives no meaning to the limitation at issue. Notably, claims 2 and 19 (from which claims 9 and 28 depend, respectively) already specify that each respective data handler is electrically connected to its associated memory device group. Netlist's interpretation is therefore redundant and ascribes no meaning to claims that concern the "position" at which a given data handler is "disposed on" a circuit board—*not* the manner in which a data handler is connected to memory devices.

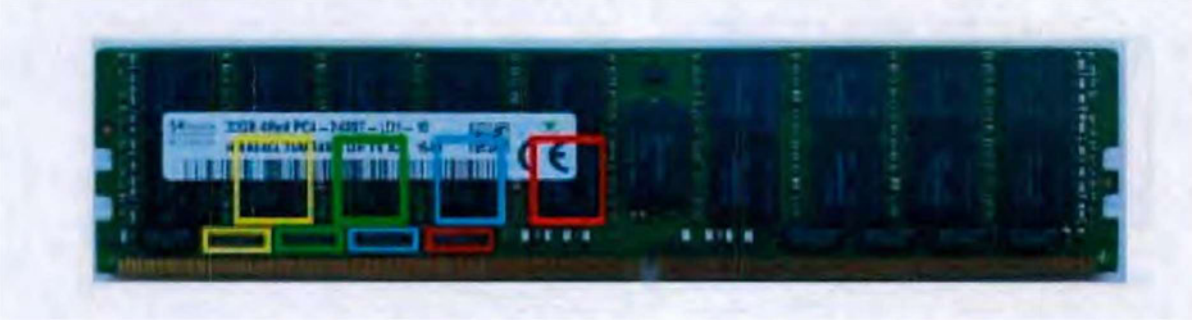
3. Netlist's Reply Position

Defendants assert that column 9, lines 22-32 "*suggests* that 'disposed on the circuit board at a position corresponding to' refers to physical proximity." *Supra* at 70 (emphasis added). The term "suggest" is a tacit admission that the specification does not clearly and unmistakably *require* their construction. *See Unwired Planet, LLC v. Apple Inc.*, 829 F.3d 1353, 1358 (Fed. Cir. 2016) ("A disclaimer or disavowal of claim scope must be clear and unmistakable, requiring 'words or expressions of manifest exclusion or restriction' in the intrinsic record."). In reality, the cited portion does not even suggest their construction. The portion discusses an embodiment where "each of the plurality of data handers 30 ***is positioned*** on the PCB 12 ***proximate to the corresponding plurality of data ports***" '523, 9:22-31. This embodiment sets out a particular example where positional correspondence is discussed in terms of proximity. But even there, the proximity is in relation to data ports and not in relation to memory devices, as Defendants argue.

Nor does the disclosure state or suggest that positional correspondence can *only* be achieved by physical proximity, as Defendants now assert.

Defendants assert that "Netlist cannot identify any other embodiment or statement in the specification that sheds light on the meaning of the disputed limitation, which claims a position." *Supra* at 71. This ignores Figure 1, which Dr. Brogioli opines would guide a POSITA as to the meaning of corresponding. Ex. 11, 2023-07-24 Brogioli Decl. In Support of Netlist's Opening Claim Construction Brief ¶ 35. In a footnote, Defendants discount Figure 1 by asserting that a POSITA would not view it as describing orientation. This is, of course, a question of fact. On one side is the testimony of Dr. Brogioli that a POSITA would understand Figure 1 to show correspondence. On the other side is no evidence, just the dictate of lawyers.

Defendants cite an ITC proceeding involving an unrelated patent but misreport Netlist's position and ignore that its holding actually undermines Defendants' position. *See supra* at 71. There, the ITC concluded that the following arrangement would satisfy the limitation's "position corresponding to" language, even though most of the respective buffer circuits are not "closest" to their corresponding memory devices. For example, the green and yellow buffers are equidistant to the yellow memory chip. And the blue buffer is closer to the green memory device than its corresponding blue memory chip. The colors are assigned based on the data lines connecting the respective buffer and chip.



Ex. 38 at 6. As such, the finding by the Commission supports Netlist's, not Defendants', position.

Defendants attempt to discount the prosecution history in which the claims were amended to remove reference to proximity as "litigation driven" is bizarre. The original claims never stated that the data handler had to be closest to a corresponding memory device, as Defendants now assert. Calling this "litigation-driven" ignores what actually transpired during the prosecution.

Corresponding is not an esoteric term. It is a common English phrase that means to match. *See, e.g.*, Ex. 46 (Merriam-Webster).

As to indefiniteness, Dr. Brogioli provides an explanation of what all of the figures in the specification depict: "each group of memory devices is connected to a data handler that is not shared with at least one other group of memory devices." Ex. 11, 2023-07-24 Brogioli Decl. ¶ 38. This construction is not "made out of whole cloth." *See supra* at 74. It describes exactly what is depicted by all embodiments in the specification.

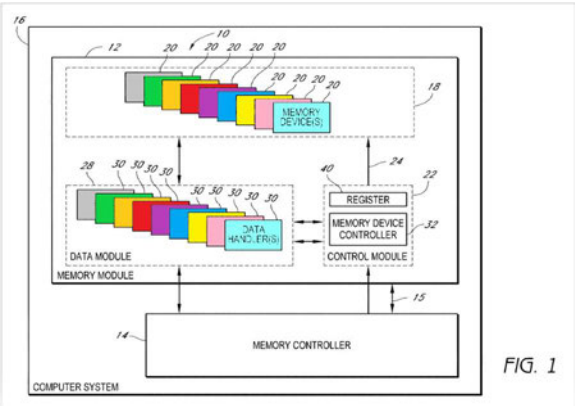


FIG. 1

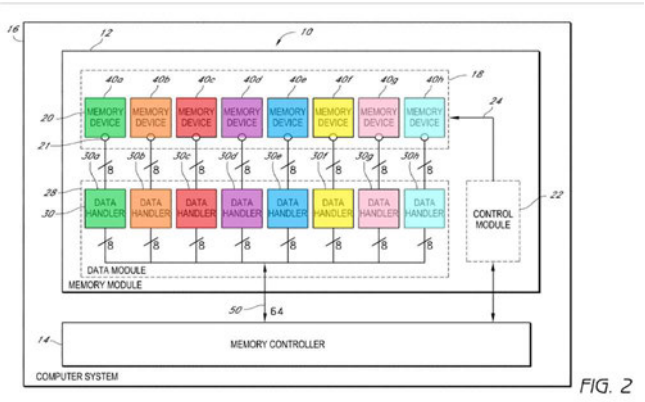


FIG. 2

Defendants have the burden of providing indefiniteness by clear and convincing evidence. *Ironburg Inventions Ltd. v. Valve Corp.*, 64 F.4th 1274, 1284 (Fed. Cir. 2023) ("[A]ny fact critical to a holding on indefiniteness . . . must be proven by the challenger by clear and convincing evidence."). They present no evidence, much less clear and convincing evidence.

4. Samsung and Google's Sur-Reply Position

The evidence is clear that Samsung and Google's construction is correct.

First, Netlist does not dispute that column 9, lines 22–31 is the only portion of the specification that describes the placement of a data handler, and it also nowhere disputes that this portion of the specification refers to the *physical* proximity of a data handler.[13] Netlist, however, insists that in this portion "proximity is in relation to data ports and not in relation memory device." This is not a serious argument; the specification, in the paragraph cited by Netlist, confirms that those data ports are the data ports *of the memory devices*. '523 patent at 9:22–31; *see also* Fig. 2 (depicting data ports 21 on each memory device 20). Netlist's contention that the specification does no more than "suggest" physical proximity is also undermined by its own expert. In a separate proceeding, Dr. Brogioli opined that "the '523 Patent's solution" to "degradation issues are reduced because 'the plurality of data handlers 30 is positioned on the PCB 12 ***proximate to*** the corresponding plurality of data ports' of the memory devices." Ex. 23, ¶ 54 (emphasis added) (citing column 9, lines 22–31). Thus, physical proximity is key to the alleged invention.

Netlist's attempts to undermine this passage are unavailing. Samsung and Google's construction is not based on an alleged disclaimer of claim scope, as Netlist's strawman posits. *Supra* at 74. Nevertheless, this is the sole disclosure informing the meaning of the disputed term, making it highly relevant to claim construction. Netlist protests that *other* portions of the '523 patent, such as Figure 1, would "guide a POSITA" as to the meaning of "corresponding," but Netlist's expert could not offer a coherent explanation for *why* Figure 1 shows "positional correspondence" at all. *See* Ex. 12 [Brogioli Tr.] at 89:19–102:20. In fact, Dr. Brogioli conceded that Figure 1 does not even depict a physical layout on a PCB, but rather "illustrates" the

[13] Netlist argues that Samsung and Google's construction is not required by the specification because, in one sentence, Samsung and Google stated that the specification "suggests" that the disputed phrase refers to physical proximity. *Supra* at 74. Netlist's argument is misguided. As set out herein, even Netlist ultimately concedes the specification discloses precisely what Samsung and Google "suggest"—physical proximity.

"functional box[es]" for "components" described in the '523 patent. *Id*. at 104:7–106:25.

Second, Netlist does not dispute that in a prior ITC action involving a different Netlist patent, Netlist argued that the phrase "each respective buffer circuit is disposed on the PCB *in a position corresponding to* the respective one or more [first and second] memory devices" requires "***physical close-ness***." Certainly, Netlist at one point understood the plain meaning of this phrase to mean physical proximity of two components. The ALJ's construction of this similar phrase, albeit for a different patent, requiring physical "alignment," supports Samsung and Google's construction because it requires a particular physical layout. Further, the ALJ construed the phrase based on the relevant disclosure in the patent, just as Samsung and Google does here.

Third, Netlist does not dispute that it certified to the Patent Office that the claim amendment involving the phrase "disposed on a circuit board at a position corresponding to" did not expand the scope of the invention beyond what is described in the specification. Ex. 8 at 12 (amendment did not add "new matter"). Netlist's present interpretation of the phrase is inconsistent with this certification. Netlist's interpretation would introduce new matter because it does not require *any* physical proximity and the '523 specification does not discuss or contemplate such a layout.

Finally, if Samsung and Google's proposed construction is not adopted, claims 9 and 28 are indefinite. A POSITA would lack the guidance required to determine whether each respective data handler is "disposed on" the circuit board "***at a position corresponding to***" the respective memory device group. Netlist's expert, Dr. Brogioli, demonstrated why the claim is indefinite during his deposition because he could not say whether numerous PCB layouts would satisfy the "disposed on the circuit board at a position corresponding to" claim language. *See* Ex. 12 [Brogioli Tr.] at 137:10–143:25; 151:6–152:10; 161:3–14; Ex. 13 [Brogioli Dep. Exs. 7–9]. Thus, if Samsung and Google's construction is rejected, claims 9 and 28 have no discernible boundaries.

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October 2, 2023

CERTIFICATE OF SERVICE

I hereby certify that on October 2, 2023, I caused the foregoing to be electronically filed with the Clerk of the Court using CM/ECF, which will send notification of such filing to all registered participants.

I further certify that I caused copies of the foregoing document to be served on October 2, 2023, upon the following in the manner indicated:

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